

Table of Contents

Opening

- The First Quartz Electronic Watch 1
Christian Piguet (Centre Suisse d'Electronique et de Microtechnique SA, Neuchâtel, Switzerland)

Arithmetics

- An Improved Power Macro-Model for Arithmetic Datapath Components .. 16
D. Helms, E. Schmidt, A. Schulz, A. Stammermann, W. Nebel (OFFIS Research Institute, Oldenburg, Germany)

- Performance Comparison of VLSI Adders Using Logical Effort 25
Hoang Q. Dao, Vojin G. Oklobdzija (University of California, USA)

- MDSP: A High-Performance Low-Power DSP Architecture 35
F. Pessolano, J. Kessels, A. Peeters (Philips Research, Eindhoven, The Netherlands)

Low-Level Modeling and Characterization

- Impact of Technology in Power-Grid-Induced Noise 45
Juan-Antonio Carballo, Sani R. Nassif (IBM Austin Research Laboratory, USA)

- Exploiting Metal Layer Characteristics for Low-Power Routing 55
Armin Windschieg, Paul Zuber, Walter Stechele (University of Technology of Munich, Germany)

- Crosstalk Measurement Technique for CMOS ICs 65
F. Picot, P. Coll (ATMEL Rousset, France), D. Auvergne (Université de Montpellier, France)

- Instrumentation Set-up for Instruction Level Power Modeling 71
S. Nikolaidis, N. Kavvadias, P. Neofotistos, K. Kosmatopoulos, T. Laopoulos (Aristotle University of Thessaloniki, Greece), L. Bisdounis (INTRACOM S.A., Peania, Greece)

Asynchronous and Adiabatic Techniques

- Low-Power Asynchronous A/D Conversion 81
Emmanuel Allier, Laurent Fesquet, Marc Renaudin, Gilles Sicard (TIMA Laboratory, Grenoble, France)

Optimal Two-Level Delay – Insensitive Implementation of Logic Functions	92
<i>Igor Lemberski, Mark Josephs (South Bank University, London, UK)</i>	

Resonant Multistage Charging of Dominant Capacitances	101
<i>Christoph Saas, Josef A. Nossek (Munich University of Technology, Germany)</i>	

A New Methodology to Design Low-Power Asynchronous Circuits	108
<i>Oscar Garnica, Juan Lanchares, Román Hermida (Universidad Complutense de Madrid, Spain)</i>	

Designing Carry Look-Ahead Adders with an Adiabatic Logic Standard-Cell Library	118
<i>Antonio Blotti, Maurizio Castellucci, Roberto Saletti (University of Pisa, Italy)</i>	

CAD Tools and Algorithms

Clocking and Clocked Storage Elements in Multi-GHz Environment	128
<i>Vojin G. Oklobdzija (University of California, USA)</i>	

Dual Supply Voltage Scaling in a Conventional Power-Driven Logic Synthesis Environment	146
<i>Torsten Mahnke, Walter Stechele (Technical University of Munich, Germany), Wolfgang Hoeld (National Semiconductor GmbH, Fuerstenfeldbruck, Germany)</i>	

Transistor Level Synthesis Dedicated to Fast I.P. Prototyping	156
<i>A. Landrault, L. Pellier, A. Richard, C. Jay (Infineon Technologies, Sophia Antipolis, France), M. Robert, D. Auvergne (LIRMM, Montpellier, France)</i>	

Robust SAT-Based Search Algorithm for Leakage Power Reduction	167
<i>Fadi A. Aloul (University of Michigan, USA), Soha Hassoun (Tufts University, USA), Karem A. Sakallah, David Blaauw (University of Michigan, USA)</i>	

Timing

PA-ZSA (Power-Aware Zero-Slack Algorithm): A Graph-Based Timing Analysis for Ultra-Low Power CMOS VLSI	178
<i>Kyu-won Choi, Abhijit Chatterjee (Georgia Institute of Technology, Atlanta, USA)</i>	

A New Methodology for Efficient Synchronization of RNS-Based VLSI Systems	188
<i>Daniel González, Antonio García (Universidad de Granada, Spain), Graham A. Jullien (University of Calgary, Canada), Javier Ramírez, Luis Parrilla, Antonio Lloris (Universidad de Granada, Spain)</i>	

Clock Distribution Network Optimization under Self-Heating and Timing Constraints	198
<i>M.R. Casu, M. Graziano, G. Masera, G. Piccinini, M.M. Prono, M. Zamboni (Politecnico di Torino, Italy)</i>	

A Technique to Generate CMOS VLSI Flip-Flops Based on Differential Latches	209
<i>Raúl Jiménez, Pilar Parra, Pedro Sanmartín, Antonio Acosta (Instituto de Microelectrónica de Sevilla, Spain)</i>	

Gate-Level Modeling

A Compact Charge-Based Propagation Delay Model for Submicronic CMOS Buffers	219
<i>José Luis Rossello, Jaume Segura (Balearic Islands University, Spain)</i>	
Output Waveform Evaluation of Basic Pass Transistor Structure	229
<i>S. Nikolaidis, H. Pournara (University of Thessaloniki, Greece), A. Chatzigeorgiou (University of Macedonia, Thessaloniki, Greece)</i>	

An Approach to Energy Consumption Modeling in RC Ladder Circuits ...	239
<i>M. Alioto (Università di Siena, Italy), G. Palumbo, M. Poli (Università di Catania, Italy)</i>	

Structure Independent Representation of Output Transition Time for CMOS Library	247
<i>P. Maurine, N. Azemard, D. Auvergne (University of Montpellier, France)</i>	

Memory Optimization

A Low Energy Clustered Instruction Memory Hierarchy for Long Instruction Word Processors	258
<i>Murali Jayapala, Francisco Barat, Pieter Op de Beeck (ESAT/ACCA, Heverlee, Belgium), Francky Catthoor (IMEC vzw, Heverlee, Belgium), Geert Deconinck, Henk Corporaal (Delft University of Technology, The Netherlands)</i>	

Design and Realization of a Low Power Register File Using Energy Model	268
<i>Xue-mei Zhao, Yi-zheng Ye (Harbin Institute of Technology, P.R. China)</i>	

Register File Energy Reduction by Operand Data Reuse	278
<i>Hiroshi Takamura, Koji Inoue, Vasily G. Moshnyaga (Fukuoka University, Japan)</i>	

Energy-Efficient Design of the Reorder Buffer.....	289
<i>Dmitry Ponomarev, Gurhan Kucuk, Kanad Ghose (State University of New York, USA)</i>	

High-Level Modeling and Design

Trends in Ultralow-Voltage RAM Technology	300
<i>Kiyoo Itoh (Central Research Laboratory, Hitachi Ltd., Tokyo, Japan)</i>	

Offline Data Profiling Techniques to Enhance Memory Compression in Embedded Systems	314
<i>Luca Benini (Università di Bologna, Italy), Alberto Macii, Enrico Macii (Politecnico di Torino, Italy)</i>	

Performance and Power Comparative Study of Discrete Wavelet Transform on Programmable Processors	323
<i>N.D. Zervas, G. Paghkless (Alma Technologies S.A., Attica, Greece), M. Dasigenis, D. Soudris (Democritus University of Thrace, Greece)</i>	

Power Consumption Estimation of a C Program for Data-Intensive Applications.....	332
<i>Eric Senn, Nathalie Julien, Johann Laurent, Eric Martin (University of South-Brittany, France)</i>	

Communications Modeling and Activity Reduction

A Low Overhead Auto-Optimizing Bus Encoding Scheme for Low Power Data Transmission	342
<i>Claudia Kretzschmar, Robert Siegmund, Dietmar Müller (Chemnitz University of Technology, Germany)</i>	

Measurement of the Switching Activity of CMOS Digital Circuits at the Gate Level.....	353
<i>C. Baena, J. Juan-Chico, M.J. Bellido, P. Ruiz de Clavijo, C.J. Jiménez, M. Valencia (Instituto de Microelectrónica de Sevilla, Spain)</i>	

Low-Power FSMs in FPGA: Encoding Alternatives	363
<i>G. Sutter, E. Todorovich (Universidad Nacional del Centro, Tandil, Argentina), S. Lopez-Buedo, E. Boemo (Universidad Autónoma de Madrid, Spain)</i>	

Synthetic Generation of Events for Address-Event-Representation Communications	371
<i>Alejandro Linares-Barranco, Gabriel Jiménez, Antón Civit (Universidad de Sevilla, Spain), Bernabé Linares-Barranco (Instituto de Microelectrónica de Sevilla, Spain)</i>	

Posters

Reducing Energy Consumption via Low-Cost Value Prediction	380
<i>Toshinori Sato, Itsujiro Arita (Kyushu Institute of Technology, Japan)</i>	

Dynamic Voltage Scheduling for Real Time Asynchronous Systems	390
<i>Mohammed Es Salhiene, Laurent Fesquet, Marc Renaudin (TIMA Laboratory, Grenoble, France)</i>	

Efficient and Fast Current Curve Estimation of CMOS Digital Circuits at the Logic Level	400
<i>Paulino Ruiz-de-Clavijo, Jorge Juan, Manuel J. Bellido, Alejandro Millán, David Guerrero (Instituto de Microelectrónica de Sevilla, Spain)</i>	

Power Efficient Vector Quantization Design Using Pixel Truncation	409
<i>Kostas Masselos, Panagiotis Merakos, Costas E. Goutis (University of Patras, Greece)</i>	

Minimizing Spurious Switching Activities in CMOS Circuits	419
<i>Artur Wróblewski, Florian Auernhammer, Josef A. Nossek (Munich University of Technology, Germany)</i>	

Modeling Propagation Delay of MUX, XOR, and D-Latch Source-Coupled Logic Gates	429
<i>M. Alioto (Università di Siena, Italy), G. Palumbo (Università di Catania, Italy)</i>	

Operating Region Modelling and Timing Analysis of CMOS Gates Driving Transmission Lines	438
<i>Gregorio Cappuccino, Giuseppe Cocorullo (University of Calabria, Italy)</i>	

Selective Clock-Gating for Low Power/Low Noise Synchronous Counters 1	448
<i>Pilar Parra, Antonio Acosta, Manuel Valencia (Instituto de Microelectrónica de Sevilla, Spain)</i>	

Probabilistic Power Estimation for Digital Signal Processing Architectures	458
<i>Achim Freimann (Universität Hannover, Germany)</i>	
Modeling of Propagation Delay of a First Order Circuit with a Ramp Input	468
<i>Rosario Mita, Gaetano Palumbo (University of Catania, Italy)</i>	
Characterization of Normal Propagation Delay for Delay Degradation Model (DDM)	477
<i>Alejandro Millán, Jorge Juan, Manuel J. Bellido, Paulino Ruiz-de-Clavijo, David Guerrero (Instituto de Microelectrónica de Sevilla, Spain)</i>	
Automated Design Methodology for CMOS Analog Circuit Blocks in Complex Systems	487
<i>Razvan Ionita (Polytechnic Institute, Bucharest, Romania), Andrei Vladimirescu (University of California, USA), Paul Jespers (Universite Catholique de Louvain, Belgium)</i>	
Author Index	495