

Table of Contents

Keynote Address

- The Age of Adaptive Computing Is Here 1
P. Master

Trends

- Disruptive Trends by Data-Stream-Based Computing 4
R. Hartenstein
- Multithreading for Logic-Centric Systems 5
G. Brebner

Rapid Prototyping

- Fast Prototyping with Co-operation of Simulation and Emulation 15
S.B. Sarmadi, S.G. Miremadi, G. Asadi, A.R. Ejlali
- How Fast Is Rapid FPGA-based Prototyping: Lessons and Challenges from the Digital TV Design Prototyping Project 26
H. Krupnova, V. Meurou, C. Barnichon, C. Serra, F. Morsi

FPGA Synthesis

- Implementing Asynchronous Circuits on LUT Based FPGAs 36
Q.T. Ho, J.-B. Rigaud, L. Fesquet, M. Renaudin, R. Rolland
- A Technique for FPGA Synthesis Driven by Automatic Source Code Analysis and Transformations 47
B. Di Martino, N. Mazzocca, G.P. Saggese, A.G.M. Strollo

Custom Computing Engines

- Flexible Routing Architecture Generation for Domain-Specific Reconfigurable Subsystems 59
K. Compton, A. Sharma, S. Phillips, S. Hauck
- iPACE-V1: A Portable Adaptive Computing Engine for Real Time Applications 69
J. Khan, M. Handa, R. Vemuri
- Field-Programmable Custom Computing Machines – A Taxonomy – 79
M. Sima, S. Vassiliadis, S. Cotofana, J.T.J. van Eijndhoven, K. Vissers

DSP Applications 1

Embedded Reconfigurable Logic Core for DSP Applications	89
<i>K. Leijten-Nowak, J.L. van Meerbergen</i>	
Efficient FPGA-based QPSK Demodulation Loops: Application to the DVB Standard	102
<i>F. Cardells-Tormo, J. Valls-Coquillat, V. Almenar-Terre, V. Torres-Carot</i>	
FPGA QAM Demodulator Design.....	112
<i>C. Dick, F. Harris</i>	

Reconfigurable Fabrics

Analytical Framework for Switch Block Design	122
<i>G.G. Lemieux, D.M. Lewis</i>	
Modular, Fabric-Specific Synthesis for Programmable Architectures	132
<i>A. Koorapaty, L. Pileggi</i>	
On Optimum Designs of Universal Switch Blocks	142
<i>H. Fan, J. Liu, Y.-L. Wu, C.-C. Cheung</i>	

Dynamic Reconfiguration 1

Improved Functional Simulation of Dynamically Reconfigurable Logic	152
<i>I. Robertson, J. Irvine, P. Lysaght, D. Robinson</i>	
Run-Time Reconfiguration to Check Temperature in Custom Computers: An Application of JBits Technology	162
<i>S. Lopez-Buedo, P. Riviere, P. Pernas, E. Boemo</i>	
Dynamic Reconfiguration in Mobile Systems.....	171
<i>G.J.M. Smit, P.J.M. Havinga, L.T. Smit, P.M. Heysters, M.A.J. Rosien</i>	
Using PARBIT to Implement Partial Run-Time Reconfigurable Systems ..	182
<i>E.L. Horta, J.W. Lockwood, S.T. Kofuji</i>	

DSP Applications 2

Multiplier-less Realization of a Poly-phase Filter Using LUT-based FPGAs	192
<i>R.H. Turner, R. Woods, T. Courtney</i>	
Speech Recognition on an FPGA Using Discrete and Continuous Hidden Markov Models	202
<i>S.J. Melnikoff, S.F. Quigley, M.J. Russell</i>	

FPGA Implementation of the Wavelet Packet Transform for High Speed communications	212
---	-----

A. Jamin, P. Mähönen

A Method for Implementing Bit-Serial Finite Impulse Response Digital Filters in FPGAs Using JBits TM	222
---	-----

A. Carreira, T.W. Fox, L.E. Turner

Routing & Placement

Automatic Partitioning for Improved Placement and Routing in Complex Programmable Logic Devices	232
---	-----

V. Manohararajah, T. Borer, S.D. Brown, Z. Vranesic

Rapid and Reliable Routability Estimation for FPGAs.....	242
--	-----

P. Kannan, S. Balachandran, D. Bhatia

Integrated Iterative Approach to FPGA Placement	253
---	-----

M. Daněk, Z. Muzikář

TDR: A Distributed-Memory Parallel Routing Algorithm for FPGAs	263
--	-----

L.A.F. Cabral, J.S. Aude, N. Maculan

Dynamic Reconfiguration 2

High-Level Partitioning of Digital Systems Based on Dynamically Reconfigurable Devices	271
--	-----

R. Kielbik, J.M. Moreno, A. Napieralski, G. Jablonski, T. Szymanski

High Speed Homology Search Using Run-Time Reconfiguration	281
---	-----

Y. Yamaguchi, Y. Miyajima, T. Maruyama, A. Konagaya

Partially Reconfigurable Cores for Xilinx Virtex	292
--	-----

M. Dyer, C. Plessl, M. Platzner

On-line Defragmentation for Run-Time Partially Reconfigurable FPGAs ..	302
--	-----

M.G. Gericota, G.R. Alves, M.L. Silva, J.M. Ferreira

Power Estimation

A Flexible Power Model for FPGAs	312
--	-----

K.K.W. Poon, A. Yan, S.J.E. Wilton

A Clocking Technique with Power Savings in Virtex-Based Pipelined Designs	322
---	-----

O. Cadenas, G. Megson

Energy Evaluation on a Reconfigurable, Multimedia-Oriented Wireless Sensor	332
--	-----

M. Martina, G. Masera, G. Piccinini, F. Vacca, M. Zamboni

A Tool for Activity Estimation in FPGAs	340
<i>E. Todorovich, M. Gilabert, G. Sutter, S. Lopez-Buedo, E. Boemo</i>	

Synthesis Issues

FSM Decomposition for Low Power in FPGA.....	350
<i>G. Sutter, E. Todorovich, S. Lopez-Buedo, E. Boemo</i>	
Hybrid Routing for FPGAs by Integrating Boolean Satisfiability with Geometric Search	360
<i>G.-J. Nam, K. Sakallah, R. Rutenbar</i>	

A Prolog-Based Hardware Development Environment	370
<i>K. Benkrid, D. Crookes, A. Benkrid, S. Belkacemi</i>	

Fly – A Modifiable Hardware Compiler	381
<i>C.H. Ho, P.H.W. Leong, K.H. Tsoi, R. Ludewig, P. Zipf, A.G. Ortiz, M. Glesner</i>	

Keynote Address

Challenges and Opportunities for FPGA Platforms	391
<i>Ivo Bolsens</i>	

Communication Applications 1

Design and Implementation of FPGA Circuits for High Speed Network Monitors	393
<i>M. Kirimura, Y. Takamoto, T. Mori, K. Yasumoto, A. Nakata, T. Higashino</i>	

Granidt: Towards Gigabit Rate Network Intrusion Detection Technology ..	404
<i>M. Gokhale, D. Dubois, A. Dubois, M. Boorman, S. Poole, V. Hogsett</i>	

New Technologies

Fast SiGe HBT BiCMOS FPGAs with New Architecture and Power Saving Techniques	414
<i>K. Zhou, Channakeshav, J.-R. Guo, C. You, B.S. Goda, R.P. Kraft, J.F. McDonald</i>	

Field–Programmable Analog Arrays: A Floating-Gate Approach	424
<i>T.S. Hall, P. Hasler, D.V. Anderson</i>	

Reconfigurable Architectures

A Generalized Execution Model for Programming on Reconfigurable Architectures and an Architecture Supporting the Model	434
<i>K. Tanigawa, T. Hironaka, A. Kojima, N. Yoshida</i>	

A Framework for Teaching (Re)Configurable Architectures in Student Projects	444
---	-----

T. Pionteck, P. Zipf, L.D. Kabulepa, M. Glesner

Communication Applications 2

Specialized Hardware for Deep Network Packet Filtering	452
--	-----

Y.H. Cho, S. Navab, W.H. Mangione-Smith

Implementation of a Successive Erasure BCH(16,7,6) Decoder and Performance Simulation by Rapid Prototyping	462
--	-----

T. Buerner

Fast RNS FPL-based Communications Receiver Design and Implementation	472
--	-----

J. Ramírez, A. García, U. Meyer-Baese, A. Lloris

Multimedia Applications

UltraSONIC: A Reconfigurable Architecture for Video Image Processing ..	482
---	-----

S.D. Haynes, H.G. Epsom, R.J. Cooper, P.L. McAlpine

Implementing the Discrete Cosine Transform Using the Xilinx Virtex FPGA	492
---	-----

T.W. Fox, L.E. Turner

Implementation of the JPEG 2000 Standard on a Virtex 1000 FPGA	503
--	-----

A. Staller, P. Dillinger, R. Männer

FPGA-based Arithmetic 1

Small Multiplier-Based Multiplication and Division Operators for Virtex-II Devices	513
--	-----

J.-L. Beuchat, A. Tisserand

Automating Customisation of Floating-Point Designs	523
--	-----

A.A. Gaffar, W. Luk, P.Y.K. Cheung, N. Shirazi, J. Hwang

Energy-Efficient Matrix Multiplication on FPGAs	534
---	-----

J.-w. Jang, S. Choi, V.K. Prasanna

Reconfigurable Processors

Run-Time Adaptive Flexible Instruction Processors	545
---	-----

S. Seng, W. Luk, P.Y.K. Cheung

DARP – A Digital Audio Reconfigurable Processor	556
---	-----

J.T. de Sousa, F.M. Gonçalves, N. Barreiro, J. Moura

System-Level Modelling for Performance Estimation of Reconfigurable Coprocessors	567
<i>S. Charlwood, J. Mangnall, S. Quigley</i>	

An FPGA Based SHA-256 Processor	577
<i>K.K. Ting, S.C.L. Yuen, K.H. Lee, P.H.W. Leong</i>	

Testing & Fault-Tolerance

Handling FPGA Faults and Configuration Sequencing Using a Hardware Extension	586
<i>P. Zipf, M. Glesner, C. Bauer, H. Wojtkowiak</i>	

On the Set of Target Path Delay Faults in Sequential Subcircuits of LUT-based FPGAs	596
<i>A. Krasniewski</i>	

Simulation-Based Analysis of SEU Effects on SRAM-based FPGAs	607
<i>M. Rebaudengo, M. Sonza Reorda, M. Violante</i>	

Exploiting Reconfigurability for Effective Testing of Delay Faults in Sequential Subcircuits of LUT-based FPGAs	616
<i>A. Krasniewski</i>	

FPGA-based Arithmetic 2

Logarithmic Number System and Floating-Point Arithmetics on FPGA ..	627
<i>R. Matoušek, M. Tichý, Z. Pohl, J. Kadlec, C. Softley, N. Coleman</i>	

Novel Optimizations for Hardware Floating-Point Units in a Modern FPGA Architecture	637
<i>E. Roesler, B. Nelson</i>	

Morphable Multipliers	647
<i>S. Chiricescu, M. Schuette, R. Glinton, H. Schmit</i>	

A Library of Parameterized Floating-Point Modules and Their Use	657
<i>P. Belanović, M. Leeser</i>	

Reconfigurable Systems

Wordlength as an Architectural Parameter for Reconfigurable Computing Devices	667
<i>T. Stansfield</i>	

An Enhanced POLIS Framework for Fast Exploration and Implementation of I/O Subsystems on CSoC Platforms	677
<i>M. Baleani, M. Conti, A. Ferrari, V. Frascola, A. Sangiovanni-Vincentelli</i>	

Introducing ReConfigME: An Operating System for Reconfigurable Computing	687
--	-----

G.B. Wigley, D.A. Kearney, D. Warren

Efficient Metacomputation Using Self-Reconfiguration	698
--	-----

R. Sidhu, V.K. Prasanna

Image Processing

An FPGA Co-processor for Real-Time Visual Tracking	710
--	-----

M. Arias-Estrada, E. Rodríguez-Palacios

Implementation of 3-D Adaptive LUM Smoother in Reconfigurable Hardware	720
---	-----

V. Fischer, M. Drutarovský, R. Lukac

Custom Coprocessor Based Matrix Algorithms for Image and Signal Processing	730
---	-----

A. Amira, A. Bouridane, P. Milligan, F. Bensaali

Parallel FPGA Implementation of the Split and Merge Discrete Wavelet Transform	740
---	-----

N. Aranki, A. Moopenn, R. Tawel

Crypto Applications 1

Fully Parameterizable Elliptic Curve Cryptography Processor over GF(2^m)	750
---	-----

T. Kerins, E. Popovici, W. Marnane, P. Fitzpatrick

6.78 Gigabits per Second Implementation of the IDEA Cryptographic Algorithm	760
--	-----

A. Hämäläinen, M. Tommiska, J. Skyttä

Rijndael Cryptographic Engine on the UltraSONIC Reconfigurable Platform	770
--	-----

E.A. Moreira, P.L. McAlpine, S.D. Haynes

A Cryptanalytic Time-Memory Tradeoff: First FPGA Implementation	780
---	-----

*J.-J. Quisquater, F.-X. Standaert, G. Rouvroy, J.-P. David,
J.-D. Legat*

Keynote Address

Creating a World of Smart Re-configurable Devices	790
---	-----

Rudy Lauwereins

Multitasking

- Interconnection Networks Enable Fine-Grain Dynamic Multi-tasking
on FPGAs 795
T. Marescaux, A. Bartic, D. Verkest, S. Vernalde, R. Lauwereins

- Multitasking Hardware on the SLAAC1-V Reconfigurable Computing
System 806
W.J. Landaker, M.J. Wirthlin, B.L. Hutchings

Special Architectures

- The Case for Fine-Grained Re-configurable Architectures: An Analysis
of Conceived Performance 816
T. Valtonen, J. Isoaho, H. Tenhunen

- An FPGA Implementation of a Multi-comparand Multi-search
Associative Processor 826
Z. Kokosiński, W. Sikora

Crypto Applications 2

- AES Implementation on FPGA: Time - Flexibility Tradeoff 836
A. Labb  , A. P  rez

- An FPGA Implementation of the Linear Cryptanalysis 845
*F. Koeune, G. Rouvroy, F.-X. Standaert, J.-J. Quisquater,
J.-P. David, J.-D. Legat*

Compilation Techniques

- Compiling Application-Specific Hardware 853
M. Budiu, S.C. Goldstein

- XPP-VC: A C Compiler with Temporal Partitioning for the
PACT-XPP Architecture 864
J.M.P. Cardoso, M. Weinhardt

- Sea Cucumber: A Synthesizing Compiler for FPGAs 875
J.L. Tripp, P.A. Jackson, B.L. Hutchings

DSP Applications 3

- Practical Considerations in the Synthesis of High Performance Digital
Filters for Implementation on FPGAs 886
J.E. Carletta, M.D. Rayman

- Low Power High Speed Algebraic Integer Frequency Sampling Filters
Using FPLDs 897
U. Meyer-Baese, J. Ram  ez, A. Garc  a

High Performance Quadrature Digital Mixers for FPGAs	905
<i>F. Cardells-Tormo, J. Valls-Coquillat</i>	

Complex Applications

HAGAR: Efficient Multi-context Graph Processors	915
<i>O. Mencer, Z. Huang, L. Huelsbergen</i>	

Scalable Implementation of the Discrete Element Method on a Reconfigurable Computing Platform	925
<i>B. Carrión Schäfer, S.F. Quigley, A.H.C. Chan</i>	

On Computing Transitive-Closure Equivalence Sets Using a Hybrid GA-DP Approach	935
<i>K.-P. Lam, S.-T. Mak</i>	

Architecture Implementation

REFLIX: A Processor Core for Reactive Embedded Applications	945
<i>Z. Salcic, P. Roop, M. Biglari-Abhari, A. Bigdeli</i>	

Factors Influencing the Performance of a CPU-RFU Hybrid Architecture	955
<i>G. Venkataramani, S. Sudhir, M. Budiu, S.C. Goldstein</i>	

Implementing Converters in FPLD	966
<i>A. Sanz, J.I. García-Nicolás, I. Urriza</i>	

A Quantitative Understanding of the Performance of Reconfigurable Coprocessors	976
<i>D. Benitez</i>	

Design Flow

Integration of Reconfigurable Hardware into System-Level Design	987
<i>K. Buchenrieder, U. Nageldinger, A. Pyttel, A. Sedlmeier</i>	

A Retargetable Macro Generation Method for the Evaluation of Repetitive Configurable Architectures	997
<i>F. Wolz, R. Kolla</i>	

The Integration of SystemC and Hardware-Assisted Verification	1007
<i>R. Ramaswamy, R. Tessier</i>	

Using Design Hierarchy to Improve Quality of Results in FPGAs	1017
<i>A.S. Kaviani</i>	

Miscellaneous

Architecture Design of a Reconfigurable Multiplier for Flexible Coarse-Grain Implementations	1027
<i>G. Koutroumpezis, K. Tatas, D. Soudris, S. Blionas, K. Masselos, A. Thanailakis</i>	
A General Hardware Design Model for Multicontext FPGAs	1037
<i>N. Kaneko, H. Amano</i>	
Dynamically Reconfigurable Hardware – A New Perspective for Neural Network Implementations	1048
<i>M. Porrmann, U. Witkowski, H. Kalte, U. Rückert</i>	
A Compilation Framework for a Dynamically Reconfigurable Architecture	1058
<i>R. David, D. Chillet, S. Pillement, O. Sentieys</i>	

Short Papers

Data Dependent Circuit for Subgraph Isomorphism Problem	1068
<i>S. Ichikawa, S. Yamamoto</i>	
Exploration of Design Space in ECDSA	1072
<i>J. Schmidt, M. Novotný, M. Jäger, M. Bečvář, M. Jáchim</i>	
2D and 3D Computer Graphics Algorithms under MORPHOSYS	1076
<i>I. Damaj, S. Majzoub, H. Diab</i>	
A HIPERLAN/2 - IEEE 802.11a Reconfigurable System-on-Chip	1080
<i>S. Blionas, K. Masselos, C. Dre, C. Drosos, F. Ieromnimon, T. Pagonis, A. Pneymatikakis, A. Tatsaki, T. Trimis, A. Vontzalidis, D. Metafas</i>	
SoftTOTEM: An FPGA Implementation of the TOTEM Parallel Processor	1084
<i>S. McBader, L. Clementel, A. Sartori, A. Boni, P. Lee</i>	
Real-Time Medical Diagnosis on a Multiple FPGA-based System	1088
<i>T. Yokota, M. Nagafuchi, Y. Mekada, T. Yoshinaga, K. Ootsu, T. Baba</i>	
Threshold Element-Based Symmetric Function Generators and Their Functional Extension	1092
<i>K. Aoyama, H. Sawada</i>	
Hardware Implementation of a Multiuser Detection Scheme Based on Recurrent Neural Networks	1097
<i>W. Schlecker, A. Engelhart, W.G. Teich, H.-J. Pfleiderer</i>	

Building Custom FIR Filters Using System Generator	1101
<i>J. Hwang, J. Ballagh</i>	
SoC Based Low Cost Design of Digital Audio Broadcasting Transport Network Applications	1105
<i>K. Feske, G. Heinrich, B. Fritzsche, M. Langer</i>	
Dynamic Constant Coefficient Convolvers Implemented in FPGAs	1110
<i>E. Jamro, K. Wiatr</i>	
VIZARD II: An FPGA-based Interactive Volume Rendering System	1114
<i>U. Kanus, G. Wetekam, J. Hirche, M. Meißner</i>	
RHiNET/NI: A Reconfigurable Network Interface for Cluster Computing	1118
<i>N. Izu, T. Yokoyama, J. Tsuchiya, K. Watanabe, H. Amano</i>	
General Purpose Prototyping Platform for Data-Processor Research and Development	1122
<i>F. Miletić, R. van Leuken, A. de Graaf</i>	
High Speed Computation of Three Dimensional Cellular Automata with FPGA	1126
<i>T. Kobori, T. Maruyama</i>	
SOPC-based Embedded Smart Strain Gage Sensor	1131
<i>S. Poussier, H. Rabah, S. Weber</i>	
Adding Hardware Support to the HotSpot Virtual Machine for Domain Specific Applications	1135
<i>Y. Ha, R. Hipik, S. Vernalde, D. Verkest, M. Engels, R. Lauwereins, H. De Man</i>	
An FPGA-based Node Controller for a High Capacity WDM Optical Packet Network	1139
<i>R. Gaudino, V. De Feo, M. Chiaberge, C. Sansoè</i>	
FPGA and Mixed FPGA-DSP Implementations of Electrical Drive Algorithms	1144
<i>F. Calmon, M. Fathallah, P.J. Viverge, C. Gontrand, J. Carrabina, P. Foussier</i>	
Image Registration of Real-Time Broadcast Video Using the UltraSONIC Reconfigurable Computer	1148
<i>W.J.C. Melis, P.Y.K. Cheung, W. Luk</i>	
A Novel Watermarking Technique for LUT Based FPGA Designs	1152
<i>D. Carline, P. Coulton</i>	

XXII Table of Contents

Implementing CSAT Local Search on FPGAs	1156
<i>M. Henz, E. Tan, R.H.C. Yap</i>	
A Reconfigurable Processor Architecture	1160
<i>A. Niyonkuru, G. Eggers, H.C. Zeidler</i>	
A Reconfigurable System-on-Chip-Based Fast EDM Process Monitor	1164
<i>S. Friebe, S. Köhler, R.G. Spallek, H. Juhr, K. Künanz</i>	
Gene Matching Using JBits	1168
<i>S.A. Guccione, E. Keller</i>	
Massively Parallel/Reconfigurable Emulation Model for the D-algorithm .	1172
<i>D.G. Saab, F. Kocan, J.A. Abraham</i>	
A Placement/Routing Approach for FPGA Accelerators	1177
<i>A. Miyashita, T. Fujiwara, T. Maruyama</i>	
Author Index	1183