

Preface

This workshop was a continuation of the PCRCW '94 workshop that focused on issues in parallel communication and routing in support of parallel processing. The workshop series provides a forum for researchers and designers to exchange ideas with respect to challenges and issues in supporting communication for high-performance parallel computing.

Within the last few years we have seen the scope of interconnection network technology expand beyond traditional multiprocessor systems to include high-availability clusters and the emerging class of system area networks. New application domains are creating new requirements for interconnection network services, e.g., real-time video, on-line data mining, etc. The emergence of quality-of-service guarantees within these domains challenges existing approaches to interconnection network design. In the recent past we have seen the emphasis on low-latency software layers, the application of multicomputer interconnection technology to distributed shared-memory multiprocessors and LAN interconnects, and the shift toward the use of commodity clusters and standard components. There is a continuing evolution toward powerful and inexpensive network interfaces, and low-cost, high-speed routers and switches from commercial vendors. The goal is to address the above issues in the context of networks of workstations, multicomputers, distributed shared-memory multiprocessors, and traditional tightly-coupled multiprocessor interconnects.

The PCRCW '97 workshop presented 20 regular papers and two short papers covering a range of topics dealing with modern interconnection networks. It was hosted by the Georgia Institute of Technology and sponsored by the Atlanta Chapter of the IEEE Computer Society.

We would like to thank the program committee members for their time and effort in organizing this workshop, and the reviewers for ensuring timely reviews under a very short time-line. We are grateful to L. Ni for the use of his web-based review system and D. Panda and C. Stunkel for enhancements to the same. These systems considerably simplified the review process. We are grateful to the efforts of Diana Fouts and D. Schimmel for the production of the proceedings. Special thanks are due to D. Fouts, Pam Halverson, and the Georgia Tech Department of Continuing Education for their contribution in handling the local arrangements and the numerous details.

As the result of the efforts of many people, we hope you find the workshop proceedings informative, stimulating, and useful in your endeavors.

June 1997

Sudhakar Yalamanchili and José Duato

Program Committee

Sudhakar Yalamanchili

Georgia Institute of Technology (Co-Chair)

José Duato

Universidad Politécnica de Valencia (Co-Chair)

Kevin Bolding

Seattle Pacific University

Rajendra Boppana

University of Texas at San Antonio

Suresh Chalasani

University of Wisconsin

Michael Galles

Silicon Graphics, Inc.

Lionel Ni

Michigan State University

Dhabaleswar K. Panda

Ohio State University

Timothy Pinkston

University of Southern California

David Schimmel

Georgia Institute of Technology

Kang G. Shin

University of Michigan

Larry Snyder

University of Washington

Referees

D. P. Agrawal
K. Bolding
R. Boppana
G. Byrd
S. Chalasani
J. Duato
M. Galles
C. Hyatt
C. T. King
L. Kucera
P. Lopez
N. Mckenzie
R. Melham
W. A. Najjar
L. Ni
D. K. Panda
T. Pinkston
D. Schimmel
J. Sengupta
K. G. Shin
A. Smai
L. Snyder
L. Thorelli
D. S. Wills
S. Yalamanchili