

Table of Contents

Design Methods

- New CAD Framework Extends Simulation of
Dynamically Reconfigurable Logic 1
Robinson, D.; McGregor, G.; Lysaght, P.

- Pebble: A Language for Parametrised and Reconfigurable
Hardware Design 9
Luk, W.; McKeever, S.

- Integrated Development Environment for Logic Synthesis
Based on Dynamically Reconfigurable FPGAs 19
Sklyarov, V.; Sal Monteiro, R.; Lau, N.; Melo, A.; Oliveira, A.; Kondratjuk, K.

- Designing for Xilinx XC6200 FPGAs 29
Hartenstein, R.W.; Herz, M.; Gilbert, F.

General Aspects

- Perspectives of Reconfigurable Computing in Research,
Industry and Education 39
Becker, J.; Kirschbaum, A.; Renner, F.-M.; Glesner, M.

- Field-Programmable Logic: Catalyst for New Computing Paradigms 49
Brebner, G.

- Run-Time Management of Dynamically Reconfigurable Designs 59
Shirazi, N.; Luk, W.; Cheung, P.Y.K.

- Acceleration of Satisfiability Algorithms by Reconfigurable Hardware 69
Platzner, M.; De Micheli, G.

Prototyping / Simulation

- An Optimized Design Flow for Fast FPGA-Based Rapid Prototyping 79
Stohmann, J.; Harbich, K.; Olbrich, M.; Barke, E.

- A Knowledge-Based System for Prototyping on FPGAs 89
Krupnova, H.; Dinh, V.D.; Saucier, G.

- JVX - A Rapid Prototyping System Based on Java and FPGAs 99
Macketanz, R.; Karl, W.

- Prototyping New ILP Architectures Using FPGAs 109
Shetler, J.; Hemme, B.; Yang, C.; Hinsz, C.

Development Methods

- CAD System for ASM and FSM Synthesis 119
Baranov, S.

VIII Table of Contents

Fast Floorplanning for FPGAs	129
<i>Emmert, J.M.; Randhar, A.; Bhatia, D.</i>	
SRAM-Based FPGAs: A Fault Model for the Configurable Logic Modules	139
<i>Renovell, M.; Portal, J.M.; Figueiras, J.; Zorian, Y.</i>	
Reconfigurable Hardware as Shared Resource in Multipurpose Computers	149
<i>Haug, G.; Rosenstiel, W.</i>	
Accelerators	
Reconfigurable Computer Array: The Bridge between High Speed Sensors and Low Speed Computing	159
<i>Robinson, S.H.; Caffrey, M.P.; Dunham, M.E.</i>	
A Reconfigurable Engine for Real-Time Video Processing	169
<i>Luk, W.; Andreou, P.; Derbyshire, A.; Dupont-De-Dinechin, F.; Rice, J.; Shirazi, N.; Siganos, D.</i>	
An FPGA Implementation of a Magnetic Bearing Controller for Mechatronic Applications	179
<i>Renner, F.-M.; Becker, J.; Glesner, M.</i>	
System Architectures	
Exploiting Contemporary Memory Techniques in Reconfigurable Accelerators	189
<i>Hartenstein, R.W.; Herz, M.; Hoffmann, T.; Nageldinger, U.</i>	
Self Modifying Circuitry - A Platform for Tractable Virtual Circuitry	199
<i>Donlin, A.</i>	
REACT: Reactive Environment for Runtime Reconfiguration	209
<i>Bhatia, D.; Kannan, P.; Simha, K.S.; GajjalaPurna, K.M.</i>	
Applications (1)	
Evaluation of the XC6200-series Architecture for Cryptographic Applications	218
<i>Charlwood, S.; James-Roxby, P.</i>	
An FPGA Based Object Recognition Machine	228
<i>Zakerolhosseini, A.; Lee, P.; Horne, E.</i>	
PCI-SCI Protocol Translations: Applying Microprogramming Concepts to FPGAs	238
<i>Acher, G.; Karl, W.; Leberecht, M.</i>	
Instruction-Level Parallelism for Reconfigurable Computing	248
<i>Callahan, T.J.; Wawrzynek, J.</i>	

Hardware/Software Codesign

A Hardware/Software Co-design Environment for Reconfigurable Logic Systems	258
<i>McGregor, G.; Robinson, D.; Lysaght, P.</i>	
Mapping Loops onto Reconfigurable Architectures	268
<i>Bondalapati, K.; Prasanna, V.K.</i>	
Speed Optimization of the ALR Circuit Using an FPGA with Embedded RAM: A Design Experience	278
<i>Asaad, S.; Warren, K.</i>	

System Development

High-Level Synthesis for Dynamically Reconfigurable Hardware/Software Systems	288
<i>Kress, R.; Pyttel, A.</i>	
Dynamic Specialisation of XC6200 FPGAs by Partial Evaluation	298
<i>McKay, N.; Singh, S.</i>	
WebScope: A Circuit Debug Tool	308
<i>Guccione, S.A.</i>	

Algorithms on FPGAs

Computing Goldbach Partitions Using Pseudo-random Bit Generator Operators on a FPGA Systolic Array	316
<i>Lavenier, D.; Saouter, Y.</i>	
Solving Boolean Satisfiability with Dynamic Hardware Configurations	326
<i>Zhong, P.; Martonosi, M.; Ashar, P.; Malik, S.</i>	
Modular Exponent Realization on FPGAs	336
<i>Pöldre, J.; Tammemäe, K.; Mandre, M.</i>	
Cost Effective 2x2 Inner Product Processors	348
<i>Fehér, B.; Szedö, G.</i>	

Applications (2)

A Field-Programmable Gate-Array System for Evolutionary Computation	356
<i>Maruyama, T.; Funatsu, T.; Hoshino, T.</i>	
A Transmutable Telecom System	366
<i>Miyazaki, T.; Shirakawa, K.; Katayama, M.; Murooka, T.; Takahara, A.</i>	

Tutorial

A Survey of Reconfigurable Computing Architectures	376
<i>Radunović, B.; Milutinović, V.</i>	

Miscellaneous

A Novel Field Programmable Gate Array Architecture for High Speed Arithmetic Processing	386
<i>Miller, N.L.; Quigley, S.F.</i>	
Accelerating DTP with Reconfigurable Computing Engines	391
<i>MacVicar, D.; Singh, S.</i>	
Hardware Mapping of a Parallel Algorithm for Matrix-Vector Multiplication Overlapping Communications and Computations	396
<i>Ojeda-Guerra, C.N.; Esper-Chaín, R.; Estupiñán, M.; Macías, E.; Suárez, A.</i>	
An Interactive Datasheet for the Xilinx XC6200	401
<i>Brebner, G.</i>	
Fast Adaptive Image Processing in FPGAs Using Stack Filters	406
<i>Woolfries, N.; Lysaght, P.; Marshall, S.; McGregor, G.; Robinson, D.</i>	
Increasing Microprocessor Performance with Tightly-Coupled Reconfigurable Logic Arrays	411
<i>Sawitzki, S.; Gratz, A.; Spallek, R.G.</i>	
A High-Performance Computing Module for a Low Earth Orbit Satellite Using Reconfigurable Logic	416
<i>Bergmann, N.W.; Sutton, P.R.</i>	
Maestro-Link: A High Performance Interconnect for PC Cluster	421
<i>Yamagiwa, S.; Ono, M.; Yamazaki, T.; Kulkasem, P.; Hirota, M.; Wada, K.</i>	
A Hardware Implementation of Constraint Satisfaction Problem Based on New Reconfigurable LSI Architecture	426
<i>Shiozawa, T.; Oguri, K.; Nagami, K.; Ito, H.; Konishi, R.; Imlig, N.</i>	
A Hardware Operating System for Dynamic Reconfiguration of FPGAs	431
<i>Merino, P.; López, J.C.; Jacome, M.</i>	
High Speed Low Level Image Processing on FPGAs Using Distributed Arithmetic	436
<i>Cerro-Prada, E.; James-Roxby, P.B.</i>	
A Flexible Implementation of High-Performance FIR Filters on Xilinx FPGAs	441
<i>Do, T.-T.; Kropp, H.; Reuter, C.; Pirsch, P.</i>	
Implementing Processor Arrays on FPGAs	446
<i>Vassányi, I.</i>	
Reconfigurable Hardware - A Study in Codesign	451
<i>Holmström, S.; Sere, K.</i>	

Statechart-Based HW/SW-Codesign of a Multi-FPGA-Board and a Microprocessor	456
<i>Ackad, C.</i>	
Simulation of ATM Switches Using Dynamically Reconfigurable FPGA's	461
<i>Touhafi, A.; Brissinck, W.F.; Dirkx, E.F.</i>	
Fast Prototyping Using System Emulators	466
<i>Rissa, T.; Mäkeläinen, T.; Niittylahti, J.; Siirtola, J.</i>	
Space-efficient Mapping of 2D-DCT onto Dynamically Configurable Coarse-Grained Architectures	471
<i>Dandalis, A.; Prasanna, V.K.</i>	
XILINX4000 Architecture-Driven Synthesis for Speed	476
<i>Lemberski, I.; Ratniece, M.</i>	
The PLD-Implementation of Boolean Function Characterized by Minimum Delay	481
<i>Tomachev, V.</i>	
Reconfigurable PCI-Bus Interface (RPCI)	485
<i>Abo Shosha, A.; Reinhart, P.; Rongen, F.</i>	
Programmable Prototyping System for Image Processing	490
<i>Trost, A.; Žemva, A.; Zajc, B.</i>	
A Co-simulation Concept for an Efficient Analysis of Complex Logic Designs	495
<i>Fischer, J.; Müller, C.; Kurz, H.</i>	
Programming and Implementation of Reconfigurable Routers	500
<i>Döring, A.C.; Obelöer, W.; Lustig, G.</i>	
Virtual Instruments Based on Reconfigurable Logic	505
<i>Moure, M.J.; Valdés, M.D.; Mandado, E.</i>	
The >S<puter: Introducing a Novel Concept for Dispatching Instructions Using Reconfigurable Hardware	510
<i>Siemers, C.; Möller, D.P.F.</i>	
A 6200 Model and Editor Based on Object Technology	515
<i>Lagadec, L.; Pottier, B.</i>	
Interfacing Hardware and Software	520
<i>Eisenring, M.; Teich, J.</i>	
Generating Layouts for Self-implementing Modules	525
<i>Hwang, J.; Patterson, C.; Mohan, S.; Dellinger, E.; Mitra, S.; Wittig, R.</i>	
Author Index	531