Preface

It was our great pleasure to hold the 2nd International Symposium on Automated Technology on Verification and Analysis (ATVA) in Taipei, Taiwan, ROC, October 31–November 3, 2004. The series of ATVA meetings is intended for the promotion of related research in eastern Asia. In the last decade, automated technology on verification has become the new strength in industry and brought forward various hot research activities in both Europe and USA. In comparison, eastern Asia has been quiet in the forum. With more and more IC design houses moving from Silicon Valley to eastern Asia, we believe this is a good time to start cultivating related research activities in the region.

The emphasis of the ATVA workshop series is on various mechanical and informative techniques, which can give engineers valuable feedback to fast converge their designs according to the specifications. The scope of interest contains the following research areas: model-checking theory, theorem-proving theory, state-space reduction techniques, languages in automated verification, parametric analysis, optimization, formal performance analysis, real-time systems, embedded systems, infinite-state systems, Petri nets, UML, synthesis, tools, and practice in industry.

As a young symposium, ATVA 2004 succeeded in attracting 69 submissions from all over the world. All submissions were rigorously reviewed by three reviewers and discussed by the PC members through the network. The final program included a general symposium and three special tracks: (1) Design of secure/high-reliability networks, (2) HW/SW coverification and cosynthesis, and (3) hardware verification. The general symposium consisted of 24 regular papers and 8 short papers. The three special tracks together accepted 7 papers. The final program also included three keynote speeches by Bob Kurshan, Rajeev Alur, and Pei-Hsin Ho; and three invited speeches by Jean-Pierre Jouannaud, Tevfik Bultan, and Shaoying Liu. The symposium was also preceded by three tutorials by Bob Kurshan, Rajeev Alur, and Pei-Hsin Ho.

We want to thank the National Science Council, Ministry of Education, and Academia Sinica of Taiwan, ROC. Without their support, ATVA 2004 would not have come to reality. We thank the Department of Electrical Engineering, Center for Information and Electronics Technologies (CIET), SOC Center, and Graduate Institute of Electronic Engineering (GIEE) of National Taiwan University for their sturdy support, and we thank Synopsys, Inc. for sponsoring ATVA 2004. We thank all the tutorial–keynote speakers, invited speakers, committee members, and reviewers of ATVA 2004. Finally, we thank Mr. Rong-Shiung Wu, for his help in maintaining the webpages and compiling the proceedings, and Mr. Lin-Zan Cai, for his help in all the paperwork.

August 2004 Farn Wang

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Special Tracks

1. Design of Secure/High-Reliability Networks, Chair: Teruo Higashino
   Additonal PC members:
   Ana R. Cavalli (France) Tai-Yi Huang (Taiwan)
   Masakatsu Nishigaki (Japan) Shoji Yuen (Japan)
2. HW/SW Coverification and Cosynthesis, Chair: Pao-Ann Hsiung
   Additonal PC members:
   Rong-Guey Chang (Taiwan) Tai-Yi Huang (Taiwan)
   Jung-Yi Kuo (Taiwan) Alan Liu (Taiwan)
   Win-Bin See (Taiwan)
3. Hardware Verification, Co-chairs: Chung-Yang Huang, Bow-Yaw Wang
   Additonal PC members:
   Tai-Yi Huang (Taiwan) Masakatsu Nishigaki (Japan)

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