

Table of Contents

Invited Talks

Esterel and Jazz : Two Synchronous Languages for Circuit Design	1
<i>Gérard Berry</i>	

Design Process of Embedded Automotive Systems - Using Model Checking for Correct Specifications	2
<i>Peter Jansen</i>	

Proof of Microprocessors

A Proof of Correctness of a Processor Implementing Tomasulo's Algorithm without a Reorder Buffer	8
<i>Ravi Hosabettu, Ganesh Gopalakrishnan, Mandayam Srivas</i>	

Formal Verification of Explicitly Parallel Microprocessors	23
<i>Byron Cook, John Launchbury, John Matthews, Dick Kieburtz</i>	

Superscalar Processor Verification Using Efficient Reductions of the Logic of Equality with Uninterpreted Functions to Propositional Logic	37
<i>Miroslav Velev, Randal Bryant</i>	

Model Checking

Model Checking TLA+ Specifications	54
<i>Yuan Yu, Panagiotis Manolios, Leslie Lamport</i>	

Efficient Decompositional Model-Checking for Regular Timing Diagrams . .	67
<i>Nina Amla, E. Allen Emerson, Kedar S. Namjoshi</i>	

Vacuity Detection in Temporal Model Checking	82
<i>Orna Kupferman, Moshe Vardi</i>	

Formal Methods and Industrial Applications

Using Symbolic Model Checking to Verify the Railway Stations of Hoorn-Kersenboogerd and Heerhugowaard	97
<i>Cindy Eisner</i>	

Practical Application of Formal Verification Techniques on a Frame Mux/Demux Chip from Nortel Semiconductors	110
<i>Y.Xu, E.Cerny, A.Silburt, A.Coady, Y.Liu, P.Pownall</i>	

Efficient Verification of Timed Automata Using Dense and Discrete Time Semantics 125
Marius Bozga, Oded Maler, Stavros Tripakis

Abstraction and Compositional Techniques

From Asymmetry to Full Symmetry: New Techniques for Symmetry Reduction in Model Checking 142
E.Allen Emerson, Richard J. Trefler

Automatic Error Correction of Large Circuits Using Boolean Decomposition and Abstraction 157
Dirk W. Hoffmann, Thomas Kropf

Abstract BDDs: A Technique for Using Abstraction in Model Checking . . . 172
Edmund Clarke, Somesh Jha, Yuan Lu, Dong Wang

Theorem Proving Related Approaches

Formal Synthesis at the Algorithmic Level 187
Christian Blumenröhr, Viktor Sabelfeld

Xs Are for Trajectory Evaluation, Booleans Are for Theorem Proving. 202
Mark Aagaard, Thomas Melham, John O’Leary

Verification of Infinite State Systems by Compositional Model Checking . . 219
K.L.McMillan

Symbolic Simulation/Symbolic Traversal

Formal Verification of Designs with Complex Control by Symbolic Simulation 234
Gerd Ritter, Hans Eveking, Holger Hinrichsen

Hints to Accelerate Symbolic Traversal 250
Kavita Ravi, Fabio Somenzi

Specification Languages and Methodologies

Modeling and Checking Networks of Communicating Real-Time Processes . 265
Jürgen Ruf, Thomas Kropf

”Have I Written Enough Properties?” A Method of Comparison between Specification and Implementation 280
Sagi Katz, Orna Grumberg, Danny Geist

Program Slicing of Hardware Description Languages 298
E.Clarke, M.Fujita, S.P.Rajan, T.Reps, S.Shankar, T.Teitelbaum

Posters

Results of the Verification of a Complex Pipelined Machine Model	313
<i>Jun Sawada, Warren A. Hunt, Jr</i>	
Hazard-Freedom Checking in Speed-Independent Systems	317
<i>Husnu Yenigun, Vladimir Levin, Doron Peled, Peter Beerel</i>	
Yet Another Look at LTL Model Checking	321
<i>Klaus Schneider</i>	
Verification of Finite-State-Machine Refinements Using a Symbolic Methodology	326
<i>Stefan Hendrixx, Luc Claesen</i>	
Refinement and Property Checking in High-Level Synthesis Using Attribute Grammars	330
<i>George Economakos, George Papakonstantinou</i>	
A Systematic Incrementalization Technique and Its Application to Hardware Design	334
<i>Steven Johnson, Yanhong Liu, Yuchen Zhang</i>	
Bisimulation and Model Checking	338
<i>Kathi Fisler, Moshe Y. Vardi</i>	
Circular Compositional Reasoning about Liveness	342
<i>K.L.McMillan</i>	
Symbolic Simulation of Microprocessor Models Using Type Classes in Haskell	346
<i>Nancy A. Day, Jeffrey R. Lewis, Byron Cook</i>	
Exploiting Retiming in a Guided Simulation Based Validation Methodology	350
<i>Aarti Gupta, Pranav Ashar, Sharad Malik</i>	
Fault Models for Embedded Systems	354
<i>Jens Chr. Godskesen</i>	
Validation of Object-Oriented Concurrent Designs by Model Checking	360
<i>Klaus Schneider, Michaela Huhn, George Logothetis</i>	
Author Index	365