

Table of Contents

Invited Talk

Trends in Computing	1
<i>Mark E. Dean</i>	

Invited Paper

A Case Study in Formal Verification of Register-Transfer Logic with ACL2: The Floating Point Adder of the AMD Athlon TM Processor	3
<i>David M. Russinoff</i>	

Contributed Papers

An Algorithm for Strongly Connected Component Analysis in $n \log n$ Symbolic Steps	37
<i>Roderick Bloem, Harold N. Gabow, Fabio Somenzi</i>	
Automated Refinement Checking for Asynchronous Processes	55
<i>Rajeev Alur, Radu Grosu, Bow-Yaw Wang</i>	
Border-Block Triangular Form and Conjunction Schedule in Image Computation	73
<i>In-Ho Moon, Gary D. Hachtel, Fabio Somenzi</i>	
B2M: A Semantic Based Tool for BLIF Hardware Descriptions	91
<i>David Basin, Stefan Friedrich, Sebastian Mödersheim</i>	
Checking Safety Properties Using Induction and a SAT-Solver	108
<i>Mary Sheeran, Satnam Singh, Gunnar Stålmarek</i>	
Combining Stream-Based and State-Based Verification Techniques	126
<i>Nancy A. Day, Mark D. Aagaard, Byron Cook</i>	
A Comparative Study of Symbolic Algorithms for the Computation of Fair Cycles	143
<i>Kavita Ravi, Roderick Bloem, Fabio Somenzi</i>	
Correctness of Pipelined Machines	161
<i>Panagiotis Manolios</i>	
Do You Trust Your Model Checker?	179
<i>Wolfgang Reif, Jürgen Ruf, Gerhard Schellhorn, Tobias Vollmer</i>	
Executable Protocol Specification in ESL	197
<i>Edmund M. Clarke, S. German, Y. Lu, Helmuth Veith, D. Wang</i>	

Formal Verification of Floating Point Trigonometric Functions	217
<i>John Harrison</i>	
Hardware Modeling Using Function Encapsulation	234
<i>Jun Sawada, Warren A. Hunt, Jr.</i>	
A Methodology for the Formal Analysis of Asynchronous Micropipelines . .	246
<i>Antonio Cerone, George J. Milne</i>	
A Methodology for Large-Scale Hardware Verification	263
<i>Mark D. Aagaard, Robert B. Jones, Thomas F. Melham, John W. O’Leary, Carl-Johan H. Seger</i>	
Model Checking Synchronous Timing Diagrams	283
<i>Nina Amla, E. Allen Emerson, Robert P. Kurshan, Kedar S. Namjoshi</i>	
Model Reductions and a Case Study	299
<i>Jin Hou, Eduard Cerny</i>	
Modeling and Parameters Synthesis for an Air Traffic Management System	316
<i>Adilson Luiz Bonifácio, Arnaldo Vieira Moura</i>	
Monitor-Based Formal Specification of PCI	335
<i>Kanna Shimizu, David L. Dill, Alan J. Hu</i>	
SAT-Based Image Computation with Application in Reachability Analysis	354
<i>Aarti Gupta, Zijiang Yang, Pranav Ashar, Anubhav Gupta</i>	
SAT-Based Verification without State Space Traversal	372
<i>Per Bjesse, Koen Claessen</i>	
Scalable Distributed On-the-Fly Symbolic Model Checking	390
<i>Shoham Ben-David, Tamir Heyman, Orna Grumberg, Assaf Schuster</i>	
The Semantics of Verilog Using Transition System Combinators	405
<i>Gordon J. Pace</i>	
Sequential Equivalence Checking by Symbolic Simulation	423
<i>Gerd Ritter</i>	
Speeding Up Image Computation by Using RTL Information	443
<i>Christoph Meinel, Christian Stangier</i>	
Symbolic Checking of Signal-Transition Consistency for Verifying High-Level Designs	455
<i>Kiyoharu Hamaguchi, Hidekazu Urushihara, Toshinobu Kashiwabara</i>	
Symbolic Simulation with Approximate Values	470
<i>Chris Wilson, David L. Dill, Randal E. Bryant</i>	

A Theory of Consistency for Modular Synchronous Systems	486
<i>Randal E. Bryant, Pankaj Chauhan, Edmund M. Clarke, Amit Goel</i>	
Verifying Transaction Ordering Properties in Unbounded Bus Networks through Combined Deductive/Algorithmic Methods	505
<i>Michael Jones, Ganesh Gopalakrishnan</i>	
Visualizing System Factorizations with Behavior Tables	520
<i>Alex Tsow, Steven D. Johnson</i>	
Author Index	539