Contents

Preface

Part I Overview 1

1.1 Low Power Microelectronics: Retrospect and Prospect **3**
J. Meindl (*Proceedings of the IEEE,* April 1995).

1.2 Micropower IC **20**
E. Vittoz (*Proceedings of the IEEE European Solid State Circuits Conference,* Grenoble, September 1980).

1.3 Low-Power CMOS Digital Design **36**
A. P. Chandrakasan, S. Sheng, and R. W. Brodersen (*IEEE Journal of Solid State Circuits,* April 1992).

1.4 CMOS Scaling for High Performance and Low-Power—The Next Ten Years **47**
B. Davari, R. Dennard, and G. Shahidi (*Proceedings of the IEEE,* April 1995).

Part II Low Voltage Technologies and Circuits 59

2.1 Low-Voltage Technologies and Circuits **61**
T. Kuroda and T. Sakurai (INVITED PAPER).

SECTION 2.1 Threshold Voltage Scaling and Control 66

2.2 Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits **66**
R. M. Swanson and J. D. Meindl (*IEEE Journal of Solid-State Circuits,* April 1972).

2.3 Trading Speed for Low Power by Choice of Supply and Threshold Voltages **74**
D. Liu and C. Svensson (*IEEE Journal of Solid-State Circuits,* January 1993).

2.4 Limitation of CMOS Supply-Voltage Scaling by MOSFET Threshold-Voltage Variation **82**
S. Sun and P. Tsui (*IEEE Custom Integrated Circuits Conference,* May 1994).

SECTION 2.2 Multiple Threshold CMOS (MTCMOS) 86

2.5 1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold Voltage CMOS **86**
S. Mutoh, T. Douskei, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada (*IEEE Journal of Solid-State Circuits,* August 1995).

2.6 A 1-V Multi-Threshold Voltage CMOS DSP with an Efficient Power Management Technique for Mobile Phone Application **93**
S. Mutoh, S. Shigematsu, Y. Matsuya, H. Fukuda, and J. Yamada (*IEEE International Solid-State Circuits Conference,* February 1996).

SECTION 2.3 Substrate Bias Controlled Variable Threshold CMOS 95

2.7 50% Active-Power Saving Without Speed Degradation Using Standby Power Reduction (SPR) Circuit **95**
K. Seta, H. Hara, T. Kuroda, M. Kakumu, and T. Sakurai (*IEEE International Solid-State Circuits Conference,* February 1995).

2.8 A 0.9V, 150MHz 10mW 4mm^2, 2-D Discrete Cosine Transform Core Processor with Variable Threshold-Voltage (VT) Scheme **97**
T. Kuroda, T. Fujita, S. Mita, T. Nagamatsu, S. Yoshioka, K. Suzuki, F. Sano, M. Norishima, M. Murota, M. Kako, M. Kinugawa, M. Kakumu, and T. Sakurai (*IEEE Journal of Solid-State Circuits,* November 1996).

SECTION 2.4 Silicon-on-Insulator Based Technologies 105

2.9 SOI CMOS for Low Power Systems **105**
D. Antoniadis (INVITED PAPER).

2.10 Back Gated CMOS on SOIAS for Dynamic Threshold Voltage Control **111**
I. Yang, C. Vieri, A. P. Chandrakasan, and D. Antoniadis (*IEEE International Electron Devices Meeting (IEDM),* December 1995).

2.11 Design of Low Power CMOS/SOI Devices and Circuits for Memory and Signal Processing Applications **115**
L. Thon and G. Shahidi (INVITED PAPER).

2.12 A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operation **121**
F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. K. Ko, and C. Hu (*IEEE Electron Device Letters,* December 1994).
2.13 A 0.5V SIMOX-MTCMOS Circuit with 200ps Logic Gate **124**
T. Douseki, S. Shigematsu, Y. Tanabe, M. Harada, H. Inokawa, and T. Tsuchiya (*IEEE International Solid-State Circuits Conference,* February 1996).

Part III Efficient DC-DC Conversion and Adaptive Power Supply Systems 127

SECTION 3.1 Efficient Low Voltage DC-DC Converter Design 129
3.1 A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System **129**
A. Stratakos, S. Sanders, and R. Brodersen (*IEEE Power Electronics Specialists Conference,* 1994).
3.2 Ultra Low-Power Control Circuits for PWM Converters **137**
A. Dancy and A. Chandrakasan (CONTRIBUTED PAPER).

SECTION 3.2 Adaptive Power Supply Systems 143
3.3 A Voltage Reduction Technique for Battery Operated Systems **143**
V. von Kaenel, P. Macken, and M. Degrauwe (*IEEE Journal of Solid-State Circuits,* October 1990).
3.4 Automatic Adjustment of Threshold and Supply Voltage for Minimum Power Consumption in CMOS Digital Circuits **148**
V. von Kaenel, M. Pardoen, E. Dijkstra, and E. Vittoz (*IEEE Symposium on Low-Power Electronics,* October 1994).
3.5 Low-Power Operation Using Self-Timed Circuits and Adaptive Scaling of the Supply Voltage **150**
L. Nielsen, C. Niessen, J. Sparso, and K. van Berkel (*IEEE Transactions on VLSI Systems,* December 1994).
3.6 A Low-Power Switching Power Supply for Self-Clocked Systems **157**
G. Wei and M. Horowitz (INVITED PAPER).
3.7 Variable-Voltage Digital-Signal Processing **166**
V. Gutnik and A. Chandrakasan (CONTRIBUTED PAPER).
3.8 Scheduling for Reduced CPU Energy **177**
M. Weiser, B. Welch, A. Demers, and S. Shenker (*First Symposium on Operating Systems Design and Implementation (OSDI),* Usenix Association, 1994).

Part IV Circuit and Logic Styles 189

SECTION 4.1 Conventional Circuit and Logic Styles 191
4.1 Silicon-Gate CMOS Frequency Divider for the Electronic Wrist Watch **191**
E. Vittoz, B. Gerber, and F. Leuenberger (*IEEE Journal of Solid-State Circuits,* April 1972).
4.2 CODYMOS Frequency Dividers Achieve Low Power Consumption and High Frequency **196**
H. Oguey and E. Vittoz (*Electronics Letters,* July 1973).
4.3 Short-Circuit Dissipation of Static CMOS Circuitry and Its Impact on the Design of Buffer Circuits **198**
H. J. M. Veendrick (*IEEE Journal of Solid-State Circuits,* August 1984).
4.4 A 3.8ns CMOS 16×16 Multiplier Using Complementary Pass Transistor Logic **204**
K. Yano, T. Yamanaka, T. Nishida, M. Saitoh, K. Shimohigashi, and A. Shimizu. (*IEEE Custom Integrated Circuits Conference,* 1989).
4.5 A High-Speed, Low-Power, Swing Restored Pass-Transistor Logic Based Multiply and Accumulate Circuit for Multimedia Applications **208**
A. Parameswar, H. Hara, and T. Sakurai (*Proceedings of Custom Integrated Circuits Conference,* May 1994).
4.6 Static Power Driven Voltage Scaling and Delay Driven Buffer Sizing in Mixed Swing QuadRail for Sub-1V I/O Swings **212**
R. Krishnamurthy, I. Lys, and L. R. Carley (*International Symposium on Low-Power Electronics and Design,* August 1996).
4.7 The Power Consumption of CMOS Adders and Multipliers **218**
T. Callaway and E. Swartzlander, Jr. (INVITED PAPER).
4.8 Delay Balanced Multipliers for Low Power/Low Voltage DSP Core **225**
T. Sakuta, W. Lee, and P. T. Balsara (*IEEE Symposium on Low-Power Electronics: Digest of Technical Papers,* October 1995).
4.9 Asynchronous Does Not Imply Low Power, But, . . . **227**
K. Van Berkel, H. van Gageldonk, J. Kessels, C. Niessen, A. Peeters, M. Roncken, and R. van de Wiel (INVITED PAPER).
4.10 Latches and Flip-Flops for Low-Power Systems **233**
C. Svensson and J. Yuan (INVITED PAPER).

SECTION 4.2 Adiabatic Logic Circuits 239

4.11 Zig-Zag Path to Understanding **239**
R. Landauer (*IEEE PhysComp* '94).

4.12 A Low-Power Multiphase Circuit Technique **245**
B. Watkins (*IEEE Journal of Solid-State Circuits,* December 1967).

4.13 Asymptotically Zero Energy Split-Level Charge Recovery Logic **253**
S. Younis and T. Knight (*International Workshop on Low Power Design,* 1994).

4.14 Low Power Digital Systems Based on Adiabatic Switching Principles **259**
W. C. Athas, L. Svensson, J. G. Koller, N. Tzartzanis, and E. Y. Chou (*IEEE Trans. on VLSI Systems,* December 1994).

4.15 Adiabatic Dynamic Logic **268**
A. Dickinson and J. Denker (*IEEE Journal of Solid-State Circuits,* March 1995).

Part V Driving Interconnect 273

5.1 Sub-1-V Swing Internal Bus Architecture for Future Low-Power ULSIs **275**
Y. Nakagome, K. Itoh, M. Isoda, K. Takeuchi, and M. Aoki (*IEEE Journal of Solid-State Circuits,* April 1993).

5.2 Data-Dependent Logic Swing Internal Bus Architecture for Ultra Low-Power LSIs **281**
M. Hiraki, H. Kojima, H. Misawa, T. Akazawa, and Y. Hatano (*IEEE Journal of Solid-State Circuits,* April 1995).

5.3 An Asymptotically Zero Power Charge-Recycling Bus Architecture for Battery-Operated Ultra-High Data Rate ULSIs **287**
H. Yamauchi, H. Akamatsu, and T. Fujita (*IEEE Journal of Solid-State Circuits,* April 1995).

5.4 Bus-Invert Coding for Low Power I/O **296**
M. Stan and W. Burleson (*IEEE Trans. on VLSI Systems,* March 1995).

5.5 A Sub-CV^2 Pad Driver with 10 ns Transition Time **306**
L. J. Svensson, W. C. Athas, and R. S-C. Wen (*IEEE International Symposium on Low-Power Electronics and Design,* August 1996).

Part VI Memory Circuits 311

6.1 Reviews and Prospects of Low-Power Memory Circuits
K. Itoh (INVITED PAPER). **313**

SECTION 6.1 DRAM 318

6.2 Trends in Low-Power RAM Circuit Technologies **318**
K. Itoh, K. Sasaki, Y. Nakagome (*Proceedings of the IEEE,* April 1995).

6.3 Standby/Active Mode Logic for Sub-1V Operating ULSI Memory **338**
D. Takashima, S. Watanabe, H. Nakano, Y. Oowaki, K. Ohuchi, and H. Tango (*IEEE Journal of Solid-State Circuits,* April 1994).

6.4 A Charge Recycle Refresh for Gb-scale DRAM's in File Application **344**
T. Kawahara, Y. Kawajiri, M. Horiguchi, T. Akiba, G. Kitsukawa, T. Kure, and M. Aoki (*IEEE Journal of Solid-State Circuits,* June 1994).

SECTION 6.2 SRAM 352

6.5 A 1-V 1-Mb SRAM for Portable Equipment **352**
H. Morimura and N. Shibata (*International Symposium on Low-Power Electronics and Design,* August 1996).

6.6 A Single Bitline Cross-Point Cell Activation (SCPA) Architecture for Ultra-Low-Power SRAMs **358**
M. Ukita, S. Murakami, T. Yamagata, H. Kuriyama, Y. Nishimura, and K. Anami (*IEEE International Solid-State Circuits Conference,* February 1994).

6.7 Techniques to Reduce Power in Fast Wide Memories **360**
B. Amrutur and M. Horowitz (*Proceedings of the IEEE Symposium on Low Power Electronics,* 1994).

6.8 A 2-ns, 5-mW, Synchronous-Powered Static-Circuit Fully Associative TLB **362**
H. Higuchi, S. Tachibana, M. Minami, and T. Nagano (*IEEE Symposium on VLSI Circuits,* June 1995).

6.9 Driving Source-Line (DSL) Cell Architecture for Sub-1-V High Speed Low Power Applications **364**
H. Mizuno and T. Nagano (*IEEE Symposium of VLSI Circuits,* June 1995).

Part VII Portable Terminal Electronics 367

SECTION 7.1 General Purpose Processor Design 369

7.1 Energy Dissipation in General Purpose Microprocessors **369**
R. Gonzalez and M. Horowitz (*IEEE Journal of Solid-State Circuits,* September 1996).

7.2 Energy Efficient CMOS Microprocessor Design **376**
T. Burd and R. Brodersen (*Proceedings of the 28th Annual HICSS Conference,* January 1995).
7.3 A 160MHz 32b 0.5W CMOS RISC Microprocessor **386**
J. Montanaro, R. Witek, K. Anne, A. Black, E. Cooper, D. Dobberpuhl, P. Donahue, J. Eno, G. Hoeppner, D. Kruckemyer, T. Lee, P. Lin, L. Madden, D. Murray, M. Pearce, S. Santhanam, K. Snyder, R. Stephany, and S. Thierauf (*IEEE Journal of Solid-State Circuits,* November 1996).
7.4 A 320Mhz, 1.5mW @ 1.35V CMOS PLL for Microprocessor Clock Generation **396**
V. Von Kaenel, D. Aebischer, C. Piguet, and E. Dijkstra (*IEEE Journal of Solid-State Circuits,* November 1996).

SECTION 7.2 Dedicated and Programmable Digital Signal Processors 404
7.5 A Low-Power Chipset for a Portable Multimedia I/O Terminal **404**
A. P. Chandrakasan, A. Burstein, and R. W. Brodersen (*IEEE Journal of Solid-State Circuits,* December 1994).
7.6 A Portable Real-Time Video Decoder for Wireless Communication **418**
T. Meng, B. Gordon, and E. Tsern (INVITED PAPER).
7.7 Low Power Design of Memory Intensive Functions **433**
D. Lidsky and J. Rabaey (*IEEE Symposium on Low-Power Electronics,* 1994).
7.8 A 16b Low-Power Digital Signal Processor **435**
K. Ueda, T. Sugimura, M. Okamoto, S. Marui, T. Ishikawa, M. Sakakihara (*IEEE International Solid-State Circuits Conference,* February 1993).
7.9 A 1.8V 36mW DSP for the Half-Rate Speech CODEC **437**
T. Shiraishi, K. Kawamoto, K. Ishikawa, H. Sato, F. Asai, E. Teraoka, T. Kengaku, H. Takata, T. Tokuda, K. Nishida, and K. Saitoh (*Proceedings of the IEEE Custom Integrated Circuits Conference,* May 1996).
7.10 Design of a 1-V Programmable DSP for Wireless Communication **441**
P. Landman, W. Lee, B. Barton, S. Abiko, H. Takahashi, H. Mizuno. S. Muramatsu, K. Tashiro, M. Fusumada, L. Pham, F. Boutaud, E. Ego, G. Gallo, H. Tran, C. Lemonds, A. Shih, M. Nandakumar, B. Eklund, and I-C. Chen (INVITED PAPER).
7.11 Stage-Skip Pipeline: A Low Power Processor Architecture Using a Decoded Instruction Buffer **450**
M. Hiraki, R. Bajwa, H. Kojima, D. Gorny, K. Nitta, A. Shridhar, K. Sasaki, and K. Seki (*International Symposium on Low Power Electronics and Design,* August 1996).

Part VIII Computer Aided Design Tools 457

SECTION 8.1 Power Analysis Techniques 459
8.1 Transition Density: A New Measure of Activity in Digital Circuits **459**
F. Najm (*IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems,* February 1993).
8.2 Estimation of Average Switching Activity in Combinational and Sequential Circuits **473**
A. Ghosh, S. Devadas, K. Keutzer, and J. White (*IEEE/ACM Design Automation Conference,* June 1992).
8.3 Power Estimation for Sequential Logic Circuits **480**
C. Tsui, J. Monteiro, M. Pedram, S. Devadas, A. Despain, and B. Lin (*IEEE Trans. on VLSI Systems,* September 1995).
8.4 A Monte Carlo Approach for Power Estimation **492**
R. Burch, F. N. Najm, P. Yang, and T. Trick (*IEEE Transactions on VLSI Systems,* March 1993).
8.5 Stratified Random Sampling for Power Estimation **501**
C. -S. Ding, C. -T. Hsieh, Q. Wu, and M. Pedram (*IEEE/ACM International Conference on Computer-Aided Design,* November 1996).
8.6 A Survey of High-Level Power Estimation Techniques **508**
P. Landman (INVITED PAPER).
8.7 Activity-Sensitive Architectural Power Analysis **516**
P. Landman and J. Rabaey (*IEEE Transactions on CAD,* June 1996).
8.8 Power Analysis of Embedded Software: A First Step Towards Software Power Minimization **533**
V. Tiwari, S. Malik, and A. Wolfe (*IEEE Trans. on VLSI Systems,* December 1994).

SECTION 8.2 Power Optimization Techniques 542
8.9 Technology Mapping for Low Power **542**
V. Tiwari, P. Ashar, and S. Malik (*Proceedings of the IEEE/ACM 30th Design Automation Conference,* June 1993).
8.10 POSE: Power Optimization and Synthesis Environment **548**
S. Iman and M. Pedram (*IEEE/ACM 33rd Design Automation Conference,* June 1996).

8.11 Transformation and Synthesis of FSMs for Low-Power Gated-Clock Implementation **554**
L. Benini and G. De Micheli (*International Symposium of Low Power Design,* April 1995).
8.12 Precomputation-Based Sequential Logic Optimization for Low Power **560**
M. Alidina, J. Monteiro, S. Devadas, A. Ghosh, and M. Papaefthymiou (*Proceedings of the IEEE/ACM International Conference on Computer-Aided Design,* November 1994).
8.13 Glitch Analysis and Reduction in Register Transfer Level Power Optimization **568**
A. Raghunathan, S. Dey, and N. Jha (*IEEE/ACM 33rd Design Automation Conference,* June 1996).
8.14 Exploiting Locality for Low-Power Design **574**
R. Mehra, L. Guerra, and J. Rabaey (*Proceedings of the IEEE Custom Integrated Circuit Conference,* May 1996).
8.15 HYPER-LP: A System for Power Minimization Using Architectural Transformations **578**
A. P. Chandrakasan, M. Potkonjak, J. Rabaey, and R. W. Brodersen (*IEEE/ACM International Conference on Computer-Aided Design,* November 1992).
8.16 Variable Voltage Scheduling **582**
S. Raje and M. Sarrafzadeh (*International Symposium on Low Power Design,* April 1995).
8.17 System-Level Transformations for Low Power Data Transfer and Storage **609**
F. Catthoor, S. Wuytack, E. de Greef, F. Franssen, L. Nachtergaele, and H. Deman (INVITED PAPER).

Author Index 619

Index 623