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2003 International Workshop on Memory Technology, Design and Testing (MTDT 2003)

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Program Introduction: T. Wik, Program Chair
MTDT Message: Adit Singh, General Chair

Keynote Address

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  Christopher Hamlin, Chief Technology Officer, LSI Logic

Session 1: DRAM for Leading Edge Applications

Chair: Robert Evans, MOSAID

Session 2: Fault Analysis and Test Generation and Verification

Chair: Eric Dupont, iROC Technology

Session 3: Enhanced Testing Techniques

Chair: Christophe Frey, ST Microelectronics

Session 4: Panel: Are All the Memory BIST Challenges Solved?

Chair and Moderator: R. Dean Adams, PDAT Technologies

Panelists: Michael Niclolaidis, iROC
           Steve Pateras, Logic Vision
           Wu-Tung Cheng, Mentor Graphics
           Shahryar Arani, Virage Logic

Session 5: Memory Roadmap, Yield and Optimization

Chair: Ad van de Goor, Delft University of Technology

Session 6: Memory Design Techniques

Chair: Joerg Vollrath, Infineon Technologies

Session 7: Special Session

Panel: Embedded DRAM
Moderator: Bruce Cockburn, University of Alberta
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