
CONTENTS

<i>List of Contributors</i>	xi
<i>Preface</i>	xiii
1. Introduction	1
1.1 Why SOI?	1
1.2 What is SOI? — Structure —	2
1.3 Advantages of SOI	4
1.4 History of the Development of SOI Technology	8
1.5 Partially-Depleted (PD) and Fully-Depleted (FD) SOI MOSFETs, and Future MOSFETs.....	16
1.6 Summary	19
References	20
2. FD-SOI Device and Process Technologies	23
2.1 Introduction	23
2.2 FD-SOI Devices	24
2.2.1 Basic Features of SOI Devices	24
2.2.2 Operating Modes of SOI MOSFETs	28
2.2.3 Basic Characteristics of FD- and PD-SOI MOSFETs ...	32

2.3	Theoretical Basis of FD-SOI Device Operation:	
	DC Operation	48
2.3.1	Subthreshold Characteristics	48
2.3.2	Post-threshold Characteristics	53
2.3.3	Short-Channel Effects	57
2.4	FD-SOI CMOS Process Technology	58
2.4.1	Fabrication Process for FD-SOI CMOS Devices	58
2.4.2	Problems and Solutions in FD-SOI Process Technology	62
2.5	Summary	76
	References	77
3.	<i>Ultralow-Power Circuit Design with FD-SOI Devices</i>	83
3.1	Introduction	83
3.2	Ultralow-Power Short-Range Wireless Systems	84
3.3	Key Design Factor for Ultralow-Power LSIs	86
3.4	Ultralow-Voltage Digital-Circuit Design	89
3.4.1	Key Technologies	89
3.4.2	Estimation of Energy Reduction	93
3.5	Robustness of Ultralow-Voltage Operation	98
3.5.1	Suppression of Floating-Body Effects	98
3.5.2	Suppression of Threshold-Voltage Fluctuations due to Operating Temperature	99
3.6	Prospects and Issues in Low-Voltage Analog Circuits	102
3.6.1	Prospects	102
3.6.2	Issues	102
3.7	Technology Scaling, Analog Performance, and Performance Trend for Electrical Systems	106
3.7.1	Technology Scaling and Analog Performance	106
3.7.2	Performance Trend of Electrical Systems	107
3.8	Low-Voltage Analog Circuit	108
3.8.1	Basic Amplifier	108
3.8.2	Switches	111
3.8.3	Use of Passive Components	113

3.9	Fully-Depleted SOI Devices for Ultralow-Power Analog Circuits	114
3.9.1	Transconductance (g_m)	114
3.9.2	On-Conductance (G_{on}) of CMOS Analog Switch.....	117
3.9.3	RF Characteristics of FD-SOI Devices	119
3.10	Future Direction of RF and Mixed Signal Systems.....	122
3.11	Summary	125
	References	126
4.	<i>0.5-V MTCMOS/SOI Digital Circuits</i>	131
4.1	Introduction	131
4.2	MTCMOS/SOI Circuits	132
4.2.1	Combinational Circuits.....	132
4.2.2	Sequential Circuits	136
4.3	Adder	144
4.3.1	Carry Look-Ahead Adder.....	145
4.3.2	Carry Select Adder	151
4.4	Multiplier.....	157
4.4.1	Booth-Encoder and Wallace-Tree Multiplier	157
4.4.2	Wave-Pipelined Multiplier	163
4.5	Memory	170
4.5.1	Design of Ultralow-Voltage Memory Cell	171
4.5.2	MTCMOS/SOI SRAM Scheme	174
4.5.3	Multi- V_{th} Memory Cell	175
4.5.4	Multi- V_{th} Readout Circuit	177
4.6	Frequency Divider.....	182
4.6.1	CMOS Frequency Divider.....	182
4.6.2	ED-MOS Frequency Divider.....	187
4.6.3	ED-CMOS Frequency Divider.....	192
4.7	CPU	196
4.8	Summary	208
	References	209

5.	<i>0.5-1V MTCMOS/SOI Analog/RF Circuits</i>	213
5.1	Introduction	213
5.2	RF Building Blocks	214
5.2.1	Piezoelectric Oscillators	215
5.2.2	Voltage Reference Generator	220
5.2.3	Transmit/Receive Switches	224
5.2.4	Low-Noise Amplifiers (LNAs).....	226
5.2.5	Power Amplifiers (PAs).....	228
5.2.6	Mixers and Image-Rejection Receiver	230
5.2.7	Voltage-Controlled Oscillator (VCO).....	242
5.2.8	Limiting Amplifiers	248
5.2.9	gm-C Filters.....	250
5.3	A/D and D/A Converters	254
5.3.1	Cyclic A/D Converter	255
5.3.2	Sigma-Delta A/D Converter	264
5.3.3	Current-Steering D/A Converter.....	270
5.4	DC-DC Converter.....	276
5.4.1	Design of DC-DC Converter	276
5.4.2	Switched-Capacitor (SC)-Type Converter.....	276
5.4.3	Buck Converter.....	279
5.4.4	Applicable Zones for SC-Type and Buck Converters	283
5.4.5	On-chip Distributed Power Supplies for Ultralow-Power LSIs.....	285
5.5	I/O and ESD-Protection Circuitry for Ultralow-Power LSIs ..	291
5.5.1	Standard Interface Trends	291
5.5.2	Problems with I/O Circuits for 0.5-V/3.3-V Conversion.....	292
5.5.3	Guidelines for Design of Interface Circuits.....	293
5.5.4	Performance of I/O Circuits	297
5.5.5	ESD Protection with FD-SOI Devices	298
5.5.6	Design and Layout Requirements for ESD Protection	300
5.6	Summary	303
	References	304

6.	<i>SPICE Model for SOI MOSFETs</i>	307
6.1	Introduction	307
6.2	SPICE Model for SOI MOSFETs.....	307
6.3	Parameter Extraction	309
6.4	Example of SOI MOSFET Simulation.....	325
6.5	Summary	333
	References	334
7.	<i>Applications</i>	337
7.1	Introduction	337
7.2	1-V Bluetooth RF Transceiver and Receiver.....	338
	7.2.1 Transceiver	338
	7.2.2 Receiver.....	345
7.3	Solar-Powered, Radio-Controlled Watch	350
7.4	Batteryless Short-Range Wireless System.....	355
	7.4.1 Transmitter	355
	7.4.2 Receiver.....	360
7.5	Summary	363
	References	364
8.	<i>Prospects for FD-SOI Technology</i>	367
8.1	Introduction	367
8.2	Evolution of Nanoscale FD-SOI Devices.....	368
8.3	Device and Substrate Technologies for Ultrathin-Body SOI MOSFETs	372
	8.3.1 Ultrathin-Body SOI MOSFETs	372
	8.3.2 SOI Wafer Technologies for Future MOSFETs.....	386
	8.3.3 Design of FD-SOI MOSFETs in Sub-100-nm Regime	389
8.4	Power-Aware Electronics and Role of FD-SOI Technology ...	398
8.5	Summary	399
	References	400
	<i>Index</i>	405
