

LIST OF FIGURES	ix
LIST OF TABLES	xv
PREFACE	xvii
1 INTRODUCTION	1
1.1 Focus	1
1.2 Introduction	2
1.3 Analog Cell Layout: Important Concerns	3
1.4 Semi-Custom Analog Layout Technologies	7
1.5 Layout Strategy	13
1.6 Overview	15
2 BASIC PLACEMENT	19
2.1 Introduction	19
2.2 Simulated Annealing for Device-Level Placement	20
2.3 Basic Placement Formulation	26
2.4 KOAN Basic Placement Functionality	33
2.5 KOAN Basic Placement Results	54
2.6 Summary	62
3 TOPOLOGICAL PLACEMENT	65
3.1 Introduction	65
3.2 Modeling Topological Constraints	66
3.3 Placement for Device Matching	68
3.4 Placement for Layout Symmetry	74
3.5 Placement for System-Level Topological Constraints	92
3.6 General Implementation Issues	97

3.7	Topologically-Constrained Results	98
3.8	Summary	104
4	GEOMETRY SHARING PLACEMENT	107
4.1	Introduction	107
4.2	Geometry Sharing Optimizations in Analog VLSI Layout	108
4.3	Supporting Geometry Sharing Optimizations	112
4.4	Geometry Sharing Results	146
4.5	Placement Optimization Dynamics	154
4.6	Summary	167
5	LINE-EXPANSION ROUTING	169
5.1	Line-Expansion Routing	169
5.2	Basic Path Finding	171
5.3	Other Basic Routing Issues	181
5.4	Results	186
5.5	Summary	187
6	INTEGRATED REROUTING	189
6.1	Need for Ripup	190
6.2	Rip-up Methodologies	192
6.3	Integrated Rip-up in ANAGRAM II	194
6.4	Embedding: Controlling Rip-up/Reroute	200
6.5	Summary	216
7	SYMMETRIC ROUTING	219
7.1	Thermal Matching	219
7.2	Parametric Device Matching	220
7.3	Symmetric Placement	221
7.4	Symmetric Routing: Motivations	223
7.5	Symmetric Routing in ANAGRAM II	224
7.6	Routability Issues in Symmetric Routing	228
7.7	Results	228
7.8	Summary	229
8	CROSSTALK AVOIDANCE ROUTING	231

8.1	Crosstalk Avoidance Routing: Background	232
8.2	Crosstalk Avoidance in ANAGRAM II	233
8.3	Path Finding and Crosstalk Penalties	238
8.4	Results	248
8.5	Summary	252
9	ADDITIONAL KOAN/ANAGRAM II RESULTS	253
9.1	Introduction	253
9.2	System-Level Overview	253
9.3	Scaling Behavior	254
9.4	Additional Comparisons with Manual Layout	256
9.5	Technology Remapping	257
9.6	Fabrication Example	260
9.7	Incremental re-spacing	261
9.8	Summary	268
10	CONCLUSIONS AND FUTURE WORK	271
	BIBLIOGRAPHY	273
	INDEX	283

LIST OF FIGURES

Chapter 1

1.1	Device parasitic reduction techniques.	4
1.2	Layout coupling effects.	5
1.3	Coupling reduction techniques.	7
1.4	Semi-custom analog layout technologies	8
1.5	The macro-cell layout style.	10
1.6	Example layout of circuit <i>smallcomp</i> .	12
1.7	Analog cell-level layout system using KOAN and ANAGRAM II.	15
1.8	Layout comparison between ANAGRAM I and KOAN/ANAGRAM II.	16

Chapter 2

2.1	Basic simulated annealing placement.	25
2.2	Global placement flow revisited.	28
2.3	Layout alternatives for a three transistor current mirror.	30
2.4	Examples of module generated and dynamically merged differential pair.	31
2.5	Sample of KOAN generated device variants.	32
2.6	Generated device geometry with labels.	32
2.7	Examples of black-box device representation	34
2.8	Examples of device representation.	36
2.9	The KOAN playing field.	37
2.10	Illustration of wire-space halos.	39
2.11	Basic device moves in KOAN.	40
2.12	Illegal overlap types.	43
2.13	Alternate net length estimators.	45
2.14	Synthetic layout examples.	55
2.15	KOAN placement evolution for <i>slicing</i> example.	56

2.16	KOAN placement evolution for <i>non-slicing</i> example.	56
2.17	Schematics for circuits <i>small-opamp</i> and <i>diff-opamp</i> .	58
2.18	Circuit <i>comparator</i> schematic.	58
2.19	Digital-style layouts of <i>small-opamp</i> .	59
2.20	Digital-style layouts of <i>diff-opamp</i> .	59
2.21	Digital-style layouts of <i>comparator</i> .	60

Chapter 3

3.1	Operational transconductance amplifier <i>ota</i> .	67
3.2	Global placement flow revisited.	67
3.3	Effect of oxide thickness gradient on device matching.	70
3.4	Geometry effects on device matching.	70
3.5	Implications of matching constraints on KOAN move-set.	71
3.6	Proximity enforcement by proximity net.	72
3.7	Maximum device separation constraints.	73
3.8	Illustrations of mixed symmetric-asymmetric circuitry.	75
3.9	Symmetric placement and routing of circuit <i>diff-ota</i> .	77
3.10	Thermally symmetric placement of circuit <i>bifet-ota</i> .	78
3.11	Illustrations of mirror-symmetric placement and routing.	79
3.12	Illustrations of perfectly-symmetric placement and asymmetric routing.	80
3.13	Illustrations of self-symmetric devices and self-symmetric placement.	81
3.14	Illustrations of perfectly symmetric placement and symmetric routing.	82
3.15	Illustrations of cross-symmetric nets.	83
3.16	Symmetric device moves in KOAN.	84
3.17	Example of mirror-symmetric layout.	85
3.18	Self-symmetric devices created by KOAN.	86
3.19	Example of perfectly-symmetric layout.	88
3.20	Example of mixed asymmetric-symmetric layout.	89
3.21	Example of simple thermally-symmetric layout.	90
3.22	Example of cross-symmetric layout.	91
3.23	Example of forced aspect ratio placement.	93
3.24	Pitch matching for analog standard cell generation.	94
3.25	Example of pitch matched placement.	94

3.26	External terminal constraints.	95
3.27	Example of external terminal constraints.	96
3.28	Topologically constrained circuit <i>small-opamp</i> placed by KOAN.	100
3.29	Topologically constrained circuit <i>diff-opamp</i> placed by KOAN.	101
3.30	Topologically constrained circuit <i>comparator</i> placed by KOAN.	102

Chapter 4

4.1	Various forms of device geometry sharing.	111
4.2	Pre-generated guard-ring interfering with geometry sharing.	114
4.3	wire-space halos interfering with device geometry sharing.	115
4.4	Reduction of routed nets by geometry sharing.	116
4.5	Illustration of terminal “buried” by merging.	117
4.6	Use of protection frames in merge detection.	121
4.7	Group reshape moves showing all five possible alignments.	124
4.8	Examples of group and single device moves.	125
4.9	Interaction of group moves with symmetrically constrained devices.	126
4.10	Effect of merging on diffusion area and perimeter.	128
4.11	Placement artifacts due to center measured MST avoided by FGMST measure.	131
4.12	Interaction of merging with wire-space halos.	132
4.13	Wells and related bulk structures for a CMOS process.	135
4.14	Pre-generated substrate contacts interfering with geometry sharing.	137
4.15	Illustration of merging of abutting bulk contacts.	138
4.16	Well merging.	138
4.17	Diffusion-straps used to extend protection of bulk contacts.	140
4.18	Intermediate steps in well generation post-processing.	143
4.19	Illustration of well biasing during routing.	144
4.20	Intermediate steps in diffusion-strap generation post-processing.	147
4.21	Topologically constrained circuit <i>small-opamp</i> placed by KOAN.	148
4.22	Topologically constrained circuit <i>diff-opamp</i> placed by KOAN.	150
4.23	Topologically constrained circuit <i>comparator</i> placed by KOAN.	151
4.24	Examples of well generation for circuit <i>comparator</i> .	154
4.25	Comparison of post-placement geometry sharing to dynamic geometry sharing optimization.	155
4.26	Cascoded operational transconductance amplifier <i>cascode-ota</i> .	156

4.27	Annealing cost function and placement evolution.	158
4.28	Feedback adjustment of $\alpha_{overlap}$.	160
4.29	Move selection dynamics.	162
4.30	Cooling schedule dynamics.	163
4.31	Placement results of circuit <i>cascode-ota</i> using 11 different random seeds.	165
4.32	Repeatability of placement runs using 11 different random seeds.	166
4.33	Sample of routed results of circuit <i>cascode-ota</i> placed using different random seeds.	166

Chapter 5

5.1	Illustration of Line-Probe Routing.	170
5.2	Partial-Path Representation	175
5.3	Target Distance Estimation	176
5.4	Simple Partial-Path Expansion	179
5.5	Contact Expansion of Partial-Path	180
5.6	Design Rule Checking	181
5.7	Terminal Fracturing Example	183
5.8	Large Opamp Routing Completed to 100% without Rip-up.	187
5.9	Dense Comparator Routing Completed to only 80% without Rip-up.	188

Chapter 6

6.1	ANAGRAM I and KOAN/ANAGRAM II Comparator Layouts (to scale).	190
6.2	Trivial Rip-up Example	197
6.3	Two Net Rip-up Example (single layer).	198
6.4	Embedding Scheme Architecture.	201
6.5	No Rip-Up/Reroute.	206
6.6	Default Settings.	207
6.7	Early Rescheduling Policies.	209
6.8	3X Higher C_{ripup} 's and $Mult_{ripup}$'s.	211
6.9	Reversed Initial Routing Order.	213
6.10	Effect of Net Priority on Routing Cost.	215
6.11	Comparator Without (left,incomplete) and With Rip-up.	217
6.12	Comparator with and without rip-up.	218

Chapter 7

7.1	Configuration for Thermal Device Matching.	220
7.2	KOAN Placement Symmetry Model.	222
7.3	Symmetric KOAN/ANAGRAM II CMOS opamp layout.	223
7.4	Extension of geometrically symmetric paths.	225
7.5	Symmetric Net Example (one layer).	226
7.6	Self-Symmetric Net Example (one layer).	227
7.7	Circuit <i>comparator</i> routed with and without symmetry.	229
7.8	Larger comparator routed with and without symmetry.	230

Chapter 8

8.1	Overlap Capacitance Situation.	236
8.2	Parallel Run Situation.	237
8.3	Simple Crosstalk Avoidance Example.	239
8.4	Effect of tuning the crosstalk weights.	242
8.5	Case of Partially Overlapping Probe Segments	243
8.6	Capacitance evaluation for partially overlapping geometry.	244
8.7	Fields for partially overlapping geometry.	245
8.8	Case of Unnecessary Staircase Jogs	246
8.9	Unoptimized and Optimized Comparator Layouts.	249
8.10	Crosstalk reduction for comparator example.	250
8.11	Detail of balance node: unoptimized and optimized.	250
8.12	Legend for balance node detail.	250
8.13	SPICE simulation of extracted comparators.	251

Chapter 9

9.1	Global placement flow revisited.	254
9.2	Scaling behavior of the KOAN placer.	255
9.3	Manual versus KOAN/ANAGRAM II layout for circuit <i>comparator</i> .	258
9.4	Manual versus KOAN/ANAGRAM II layout for circuit <i>diff-opamp</i> .	259
9.5	Examples of BiMOS layout.	260
9.6	Fabricated opamp.	262
9.7	Incremental re-spacing in KOAN.	263
9.8	Re-spacing for guaranteed routability.	266

9.9 Re-spacing example.

267

9.10 Placer-Router Interaction Experiment.

269

Chapter 10