Contents

1 Introduction **1**

1.1 Motivation 1

1.2 Computation Models 3

1.2.1 Parallel Random Access Machine (PRAM) 3

1.2.2 Distributed Memory Machine (DMM) 4

1.2.3 Reconfigurable DMM (RDMM) 6

1.2.4 Reconfigurable mesh DMM (RM-DMM) 7

1.3 Criteria for the Quality of Simulations 8

1.4 Previous Work 8

1.4.1 Deterministic PRAM Simulations 9

1.4.2 Randomized PRAM Simulations 10

1.5 New Results 12

1.6 Organization 14

2 Basics **16**

2.1 Universal Hashing 16

2.2 Majority Techniques 19

2.3 Log-Star Techniques 20

3 Direct PRAM Simulations **23**

3.1 A Direct $O(\log\log n/\log\log\log n)$ Delay Simulation 23

3.2 A Lower Bound for Simple Access Protocols 33

4 Indirect PRAM Simulations **39**

4.1 The Access Graph H 39

4.2 An $O(\log\log n/\log\log\log n)$ Delay Simulation 44

4.2.1 The Neighbor-Data-Structure 44

4.2.2 Schedule and Analysis of the Simulation 45

4.3 $o(\log\log n/\log\log\log n)$ Delay Simulations 47

4.3.1 The Path-Access-Structure 48

4.3.2 Cleaning Up Connected Components 52

4.3.3 An $O(\sqrt{\log \log n} \log^* n)$ Delay Simulation 53
4.3.4 An $O(\log \log \log n \log^* n)$ Delay Simulation 55
4.4 A Lower Bound for Topological Simulations 57

5 PRAM Simulations on Reconfigurable Architectures **65**
5.1 Introduction 65
5.2 An $O(\log^* n)$ Delay Simulation on a Reconfigurable DMM . . 66
5.3 Simulation with Constant Delay on a Reconfigurable Mesh DMM 68
5.3.1 Simulation Between Reconfigurable Architectures . . . 69
5.3.2 Analysis of the Simulation on a Reconfigurable Mesh DMM 70

6 Routing on a Complete Network **73**
6.1 'All-But-Linear' Routing 73
6.2 $k - k$ Relation Routing 78

7 General tools for PRAM Simulations **85**
7.1 Reduction from CRCW PRAM to EREW PRAM 85
7.2 Time-Processor Optimal EREW PRAM Simulations 87

8 Conclusions **89**

A Inequalities **91**
A.1 Tail Estimates 91
A.2 Graph Theory 92

B Reconfigurable Meshes **93**
B.1 Constant Time Algorithms on Reconfigurable Meshes 93

Bibliography **94**