# CONTENTS


Preface xx

PART ONE
**SOLID STATE ELECTRONIC AND DEVICES 1**

CHAPTER 1
**INTRODUCTION TO ELECTRONICS 3**

1.1 A Brief History of Electronics: From Vacuum Tubes to Giga-Scale Integration 5
1.2 Classification of Electronic Signals 8
1.2.1 Digital Signals 9
1.2.2 Analog Signals 9
1.2.3 A/D and D/A Converters—Bridging the Analog and Digital Domains 10
1.3 Notational Conventions 12
1.4 Problem-Solving Approach 13
1.5 Important Concepts from Circuit Theory 15
1.5.1 Voltage and Current Division 15
1.5.2 Thévenin and Norton Circuit Representations 16
1.6 Frequency Spectrum of Electronic Signals 21
1.7 Amplifiers 22
1.7.1 Ideal Operational Amplifiers 23
1.7.2 Amplifier Frequency Response 25
1.8 Element Variations in Circuit Design 26
1.8.1 Mathematical Modeling of Tolerances 26
1.8.2 Worst-Case Analysis 27
1.8.3 Monte Carlo Analysis 29
1.8.4 Temperature Coefficients 32
1.9 Numeric Precision 34
*Summary 34*
*Key Terms 35*
*References 36*
*Additional Reading 36*
*Problems 37*

CHAPTER 2
**SOLID-STATE ELECTRONICS 42**

2.1 Solid-State Electronic Materials 44
2.2 Covalent Bond Model 45
2.3 Drift Currents and Mobility in Semiconductors 48
2.3.1 Drift Currents 48
2.3.2 Mobility 49
2.3.3 Velocity Saturation 49
2.4 Resistivity of Intrinsic Silicon 50
2.5 Impurities in Semiconductors 51
2.5.1 Donor Impurities in Silicon 52
2.5.2 Acceptor Impurities in Silicon 52
2.6 Electron and Hole Concentrations in Doped Semiconductors 52
2.6.1 *n*-Type Material ($N_D > N_A$) 53
2.6.2 *p*-Type Material ($N_A > N_D$) 54
2.7 Mobility and Resistivity in Doped Semiconductors 55
2.8 Diffusion Currents 59
2.9 Total Current 60
2.10 Energy Band Model 61
2.10.1 Electron–Hole Pair Generation in an Intrinsic Semiconductor 61
2.10.2 Energy Band Model for a Doped Semiconductor 62
2.10.3 Compensated Semiconductors 62
2.11 Overview of Integrated Circuit Fabrication 64
*Summary 67*
*Key Terms 68*
*Reference 69*
*Additional Reading 69*
*Important Equations 69*
*Problems 70*

CHAPTER 3
**SOLID-STATE DIODES AND DIODE CIRCUITS 74**

3.1 The *pn* Junction Diode 75
3.1.1 *pn* Junction Electrostatics 75
3.1.2 Internal Diode Currents 79

3.2 The *i-v* Characteristics of the Diode 80
3.3 The Diode Equation: A Mathematical Model for the Diode 82
3.4 Diode Characteristics Under Reverse, Zero, and Forward Bias 85
3.4.1 Reverse Bias 85
3.4.2 Zero Bias 85
3.4.3 Forward Bias 86
3.5 Diode Temperature Coefficient 89
3.6 Diodes Under Reverse Bias 89
3.6.1 Saturation Current in Real Diodes 90
3.6.2 Reverse Breakdown 91
3.6.3 Diode Model for the Breakdown Region 92
3.7 *pn* Junction Capacitance 92
3.7.1 Reverse Bias 92
3.7.2 Forward Bias 93
3.8 Schottky Barrier Diode 93
3.9 Diode SPICE Model and Layout 94
3.10 Diode Circuit Analysis 96
3.10.1 Load-Line Analysis 96
3.10.2 Analysis Using the Mathematical Model for the Diode 98
3.10.3 The Ideal Diode Model 102
3.10.4 Constant Voltage Drop Model 104
3.10.5 Model Comparison and Discussion 105
3.11 Multiple-Diode Circuits 106
3.12 Analysis of Diodes Operating in the Breakdown Region 109
3.12.1 Load-Line Analysis 109
3.12.2 Analysis with the Piecewise Linear Model 109
3.12.3 Voltage Regulation 110
3.12.4 Analysis Including Zener Resistance 111
3.12.5 Line and Load Regulation 112
3.13 Half-Wave Rectifier Circuits 113
3.13.1 Half-Wave Rectifier with Resistor Load 113
3.13.2 Rectifier Filter Capacitor 114
3.13.3 Half-Wave Rectifier with *RC* Load 115
3.13.4 Ripple Voltage and Conduction Interval 116
3.13.5 Diode Current 118
3.13.6 Surge Current 120
3.13.7 Peak-Inverse-Voltage (PIV) Rating 120
3.13.8 Diode Power Dissipation 120
3.13.9 Half-Wave Rectifier with Negative Output Voltage 121
3.14 Full-Wave Rectifier Circuits 123
3.14.1 Full-Wave Rectifier with Negative Output Voltage 124
3.15 Full-Wave Bridge Rectification 125
3.16 Rectifier Comparison and Design Tradeoffs 125
3.17 Dynamic Switching Behavior of the Diode 129
3.18 Photo Diodes, Solar Cells, and Light-Emitting Diodes 130
3.18.1 Photo Diodes and Photodetectors 130
3.18.2 Power Generation from Solar Cells 131
3.18.3 Light-Emitting Diodes (LEDs) 132
*Summary 133*
*Key Terms 134*
*Reference 135*
*Additional Reading 135*
*Problems 135*

**CHAPTER 4**
**FIELD-EFFECT TRANSISTORS 145**

4.1 Characteristics of the MOS Capacitor 146
4.1.1 Accumulation Region 147
4.1.2 Depletion Region 148
4.1.3 Inversion Region 148
4.2 The NMOS Transistor 148
4.2.1 Qualitative *i-v* Behavior of the NMOS Transistor 149
4.2.2 Triode Region Characteristics of the NMOS Transistor 150
4.2.3 On Resistance 153
4.2.4 Saturation of the *i-v* Characteristics 154
4.2.5 Mathematical Model in the Saturation (Pinch-Off) Region 155
4.2.6 Transconductance 157
4.2.7 Channel-Length Modulation 157
4.2.8 Transfer Characteristics and Depletion-Mode MOSFETS 158
4.2.9 Body Effect or Substrate Sensitivity 159
4.3 PMOS Transistors 161
4.4 MOSFET Circuit Symbols 163
4.5 Capacitances in MOS Transistors 165
4.5.1 NMOS Transistor Capacitances in the Triode Region 165
4.5.2 Capacitances in the Saturation Region 166
4.5.3 Capacitances in Cutoff 166
4.6 MOSFET Modeling in SPICE 167

4.7 MOS Transistor Scaling 169
4.7.1 Drain Current 169
4.7.2 Gate Capacitance 169
4.7.3 Circuit and Power Densities 170
4.7.4 Power-Delay Product 170
4.7.5 Cutoff Frequency 171
4.7.6 High Field Limitations 171
4.7.7 Subthreshold Conduction 172
4.8 MOS Transistor Fabrication and Layout Design Rules 172
4.8.1 Minimum Feature Size and Alignment Tolerance 173
4.8.2 MOS Transistor Layout 173
4.9 Biasing the NMOS Field-Effect Transistor 176
4.9.1 Why Do We Need Bias? 176
4.9.2 Constant Gate-Source Voltage Bias 178
4.9.3 Load Line Analysis for the Q-Point 181
4.9.4 Four-Resistor Biasing 182
4.10 Biasing the PMOS Field-Effect Transistor 188
4.11 The Junction Field-Effect Transistor (JFET) 190
4.11.1 The JFET with Bias Applied 191
4.11.2 JFET Channel with Drain-Source Bias 191
4.11.3 *n*-Channel JFET *i-v* Characteristics 193
4.11.4 The *p*-Channel JFET 195
4.11.5 Circuit Symbols and JFET Model Summary 195
4.11.6 JFET Capacitances 196
4.12 JFET Modeling in SPICE 197
4.13 Biasing the JFET and Depletion-Mode MOSFET 198
*Summary 200*
*Key Terms 202*
*References 203*
*Problems 204*

**CHAPTER 5**

**BIPOLAR JUNCTION TRANSISTORS 217**

5.1 Physical Structure of the Bipolar Transistor 218
5.2 The Transport Model for the *npn* Transistor 219
5.2.1 Forward Characteristics 220
5.2.2 Reverse Characteristics 222
5.2.3 The Complete Transport Model Equations for Arbitrary Bias Conditions 223
5.3 The *pnp* Transistor 225
5.4 Equivalent Circuit Representations for the Transport Models 227
5.5 The *i-v* Characteristics of the Bipolar Transistor 228
5.5.1 Output Characteristics 228
5.5.2 Transfer Characteristics 229
5.6 The Operating Regions of the Bipolar Transistor 230
5.7 Transport Model Simplifications 231
5.7.1 Simplified Model for the Cutoff Region 231
5.7.2 Model Simplifications for the Forward-Active Region 233
5.7.3 Diodes in Bipolar Integrated Circuits 239
5.7.4 Simplified Model for the Reverse-Active Region 240
5.7.5 Modeling Operation in the Saturation Region 242
5.8 Nonideal Behavior of the Bipolar Transistor 245
5.8.1 Junction Breakdown Voltages 246
5.8.2 Minority-Carrier Transport in the Base Region 246
5.8.3 Base Transit Time 247
5.8.4 Diffusion Capacitance 249
5.8.5 Frequency Dependence of the Common-Emitter Current Gain 250
5.8.6 The Early Effect and Early Voltage 250
5.8.7 Modeling the Early Effect 251
5.8.8 Origin of the Early Effect 251
5.9 Transconductance 252
5.10 Bipolar Technology and SPICE Model 253
5.10.1 Qualitative Description 253
5.10.2 SPICE Model Equations 254
5.10.3 High-Performance Bipolar Transistors 255
5.11 Practical Bias Circuits for the BJT 256
5.11.1 Four-Resistor Bias Network 258
5.11.2 Design Objectives for the Four-Resistor Bias Network 260
5.11.3 Iterative Analysis of the Four-Resistor Bias Circuit 266
5.12 Tolerances in Bias Circuits 266
5.12.1 Worst-Case Analysis 267
5.12.2 Monte Carlo Analysis 269
*Summary 272*
*Key Terms 274*
*References 274*
*Problems 275*

PART TWO
**DIGITAL ELECTRONICS 285**

CHAPTER 6
**INTRODUCTION TO DIGITAL ELECTRONICS 287**

6.1 Ideal Logic Gates 289
6.2 Logic Level Definitions and Noise Margins 289
6.2.1 Logic Voltage Levels 291
6.2.2 Noise Margins 291
6.2.3 Logic Gate Design Goals 292
6.3 Dynamic Response of Logic Gates 293
6.3.1 Rise Time and Fall Time 293
6.3.2 Propagation Delay 294
6.3.3 Power-Delay Product 294
6.4 Review of Boolean Algebra 295
6.5 NMOS Logic Design 297
6.5.1 NMOS Inverter with Resistive Load 298
6.5.2 Design of the $W/L$ Ratio of $M_S$ 299
6.5.3 Load Resistor Design 300
6.5.4 Load-Line Visualization 300
6.5.5 On-Resistance of the Switching Device 302
6.5.6 Noise Margin Analysis 303
6.5.7 Calculation of $V_{IL}$ and $V_{OH}$ 303
6.5.8 Calculation of $V_{IH}$ and $V_{OL}$ 304
6.5.9 Load Resistor Problems 305
6.6 Transistor Alternatives to the Load Resistor 306
6.6.1 The NMOS Saturated Load Inverter 307
6.6.2 NMOS Inverter with a Linear Load Device 315
6.6.3 NMOS Inverter with a Depletion-Mode Load 316
6.6.4 Static Design of the Pseudo NMOS Inverter 319
6.7 NMOS Inverter Summary and Comparison 323
6.8 NMOS NAND and NOR Gates 324
6.8.1 NOR Gates 325
6.8.2 NAND Gates 326
6.8.3 NOR and NAND Gate Layouts in NMOS Depletion-Mode Technology 327
6.9 Complex NMOS Logic Design 328
6.10 Power Dissipation 333
6.10.1 Static Power Dissipation 333
6.10.2 Dynamic Power Dissipation 334
6.10.3 Power Scaling in MOS Logic Gates 335
6.11 Dynamic Behavior of MOS Logic Gates 337
6.11.1 Capacitances in Logic Circuits 337
6.11.2 Dynamic Response of the NMOS Inverter with a Resistive Load 338
6.11.3 Pseudo NMOS Inverter 343
6.11.4 A Final Comparison of NMOS Inverter Delays 344
6.11.5 Scaling Based Upon Reference Circuit Simulation 346
6.11.6 Ring Oscillator Measurement of Intrinsic Gate Delay 346
6.11.7 Unloaded Inverter Delay 347
6.12 PMOS Logic 349
6.12.1 PMOS Inverters 349
6.12.2 NOR and NAND Gates 352
*Summary 352*
*Key Terms 354*
*References 355*
*Additional Reading 355*
*Problems 355*

CHAPTER 7
**COMPLEMENTARY MOS (CMOS) LOGIC DESIGN 367**

7.1 CMOS Inverter Technology 368
7.1.1 CMOS Inverter Layout 370
7.2 Static Characteristics of the CMOS Inverter 370
7.2.1 CMOS Voltage Transfer Characteristics 371
7.2.2 Noise Margins for the CMOS Inverter 373
7.3 Dynamic Behavior of the CMOS Inverter 375
7.3.1 Propagation Delay Estimate 375
7.3.2 Rise and Fall Times 377
7.3.3 Performance Scaling 377
7.3.4 Delay of Cascaded Inverters 379
7.4 Power Dissipation and Power Delay Product in CMOS 380
7.4.1 Static Power Dissipation 380
7.4.2 Dynamic Power Dissipation 381
7.4.3 Power-Delay Product 382
7.5 CMOS NOR and NAND Gates 384
7.5.1 CMOS NOR Gate 384
7.5.2 CMOS NAND Gates 387
7.6 Design of Complex Gates in CMOS 388
7.7 Minimum Size Gate Design and Performance 393
7.8 Dynamic Domino CMOS Logic 395
7.9 Cascade Buffers 397
7.9.1 Cascade Buffer Delay Model 397
7.9.2 Optimum Number of Stages 398
7.10 The CMOS Transmission Gate 400
7.11 CMOS Latchup 401

*Summary 404*
*Key Terms 405*
*References 406*
*Problems 406*

CHAPTER 8
MOS MEMORY AND STORAGE CIRCUITS 416

8.1 Random Access Memory 417
8.1.1 Random Access Memory (RAM) Architecture 417
8.1.2 A 256-Mb Memory Chip 418
8.2 Static Memory Cells 419
8.2.1 Memory Cell Isolation and Access—The 6-T Cell 422
8.2.2 The Read Operation 422
8.2.3 Writing Data into the 6-T Cell 426
8.3 Dynamic Memory Cells 428
8.3.1 The One-Transistor Cell 430
8.3.2 Data Storage in the 1-T Cell 430
8.3.3 Reading Data from the 1-T Cell 431
8.3.4 The Four-Transistor Cell 433
8.4 Sense Amplifiers 434
8.4.1 A Sense Amplifier for the 6-T Cell 434
8.4.2 A Sense Amplifier for the 1-T Cell 436
8.4.3 The Boosted Wordline Circuit 438
8.4.4 Clocked CMOS Sense Amplifiers 438
8.5 Address Decoders 440
8.5.1 NOR Decoder 440
8.5.2 NAND Decoder 440
8.5.3 Decoders in Domino CMOS Logic 443
8.5.4 Pass-Transistor Column Decoder 443
8.6 Read-Only Memory (ROM) 444
8.7 Flip-Flops 447
8.7.1 RS Flip-Flop 449
8.7.2 The D-Latch Using Transmission Gates 450
8.7.3 A Master-Slave D Flip-Flop 450
*Summary 451*
*Key Terms 452*
*References 452*
*Problems 453*

CHAPTER 9
BIPOLAR LOGIC CIRCUITS 460

9.1 The Current Switch (Emitter-Coupled Pair) 461
9.1.1 Mathematical Model for Static Behavior of the Current Switch 462
9.1.2 Current Switch Analysis for $v_I > V_{REF}$ 463
9.1.3 Current Switch Analysis for $v_I < V_{REF}$ 464
9.2 The Emitter-Coupled Logic (ECL) Gate 464
9.2.1 ECL Gate with $v_I = V_H$ 465
9.2.2 ECL Gate with $v_I = V_L$ 466
9.2.3 Input Current of the ECL Gate 466
9.2.4 ECL Summary 466
9.3 Noise Margin Analysis for the ECL Gate 467
9.3.1 $V_{IL}$, $V_{OH}$, $V_{IH}$, and $V_{OL}$ 467
9.3.2 Noise Margins 468
9.4 Current Source Implementation 469
9.5 The ECL OR-NOR Gate 471
9.6 The Emitter Follower 473
9.6.1 Emitter Follower with a Load Resistor 474
9.7 "Emitter Dotting" or "Wired-OR" Logic 476
9.7.1 Parallel Connection of Emitter-Follower Outputs 477
9.7.2 The Wired-OR Logic Function 477
9.8 ECL Power-Delay Characteristics 477
9.8.1 Power Dissipation 477
9.8.2 Gate Delay 479
9.8.3 Power-Delay Product 480
9.9 Current Mode Logic 481
9.9.1 CML Logic Gates 481
9.9.2 CML Logic Levels 482
9.9.3 $V_{EE}$ Supply Voltage 482
9.9.4 Higher-Level CML 483
9.9.5 CML Power Reduction 484
9.9.6 NMOS CML 485
9.10 The Saturating Bipolar Inverter 487
9.10.1 Static Inverter Characteristics 488
9.10.2 Saturation Voltage of the Bipolar Transistor 488
9.10.3 Load-Line Visualization 491
9.10.4 Switching Characteristics of the Saturated BJT 491
9.11 A Transistor-Transistor Logic (TTL) Prototype 494
9.11.1 TTL Inverter for $v_I = V_L$ 494
9.11.2 TTL Inverter for $v_I = V_H$ 495
9.11.3 Power in the Prototype TTL Gate 496
9.11.4 $V_{IH}$, $V_{IL}$, and Noise Margins for the TTL Prototype 496
9.11.5 Prototype Inverter Summary 498
9.11.6 Fanout Limitations of the TTL Prototype 498
9.12 The Standard 7400 Series TTL Inverter 500
9.12.1 Analysis for $v_I = V_L$ 500
9.12.2 Analysis for $v_I = V_H$ 501

9.12.3 Power Consumption 503
9.12.4 TTL Propagation Delay and Power-Delay Product 503
9.12.5 TTL Voltage Transfer Characteristic and Noise Margins 503
9.12.6 Fanout Limitations of Standard TTL 504
9.13 Logic Functions in TTL 504
9.13.1 Multi-Emitter Input Transistors 505
9.13.2 TTL NAND Gates 505
9.13.3 Input Clamping Diodes 506
9.14 Schottky-Clamped TTL 506
9.15 Comparison of the Power-Delay Products of ECL and TTL 508
9.16 BiCMOS Logic 508
9.16.1 BiCMOS Buffers 509
9.16.2 BiNMOS Inverters 511
9.16.3 BiCMOS Logic Gates 513
*Summary 513*
*Key Terms 515*
*References 515*
*Additional Reading 515*
*Problems 516*

PART THREE
**ANALOG ELECTRONICS 527**

CHAPTER 10
**ANALOG SYSTEMS AND IDEAL OPERATIONAL AMPLIFIERS 529**

10.1 An Example of an Analog Electronic System 530
10.2 Amplification 531
10.2.1 Voltage Gain 532
10.2.2 Current Gain 533
10.2.3 Power Gain 533
10.2.4 The Decibel Scale 534
10.3 Two-Port Models for Amplifiers 537
10.3.1 The *g*-parameters 537
10.4 Mismatched Source and Load Resistances 541
10.5 Introduction to Operational Amplifiers 544
10.5.1 The Differential Amplifier 544
10.5.2 Differential Amplifier Voltage Transfer Characteristic 545
10.5.3 Voltage Gain 545
10.6 Distortion in Amplifiers 548
10.7 Differential Amplifier Model 549
10.8 Ideal Differential and Operational Amplifiers 551
10.8.1 Assumptions for Ideal Operational Amplifier Analysis 551
10.9 Analysis of Circuits Containing Ideal Operational Amplifiers 552
10.9.1 The Inverting Amplifier 553
10.9.2 The Transresistance Amplifier—A Current-to-Voltage Converter 556
10.9.3 The Noninverting Amplifier 558
10.9.4 The Unity-Gain Buffer, or Voltage Follower 561
10.9.5 The Summing Amplifier 563
10.9.6 The Difference Amplifier 565
10.10 Frequency-Dependent Feedback 568
10.10.1 Bode Plots 568
10.10.2 The Low-Pass Amplifier 568
10.10.3 The High-Pass Amplifier 572
10.10.4 Band-Pass Amplifiers 575
10.10.5 An Active Low-Pass Filter 578
10.10.6 An Active High-Pass Filter 581
10.10.7 The Integrator 582
10.10.8 The Differentiator 586
*Summary 586*
*Key Terms 588*
*References 588*
*Additional Reading 589*
*Problems 589*

CHAPTER 11
**NONIDEAL OPERATIONAL AMPLIFIERS AND FEEDBACK AMPLIFIER STABILITY 600**

11.1 Classic Feedback Systems 601
11.1.1 Closed-Loop Gain Analysis 602
11.1.2 Gain Error 602
11.2 Analysis of Circuits Containing Nonideal Operational Amplifiers 603
11.2.1 Finite Open-Loop Gain 603
11.2.2 Nonzero Output Resistance 606
11.2.3 Finite Input Resistance 610
11.2.4 Summary of Nonideal Inverting and Noninverting Amplifiers 614
11.3 Series and Shunt Feedback Circuits 615
11.3.1 Feedback Amplifier Categories 615
11.3.2 Voltage Amplifiers—Series-Shunt Feedback 616
11.3.3 Transimpedance Amplifiers—Shunt-Shunt Feedback 616
11.3.4 Current Amplifiers—Shunt-Series Feedback 616
11.3.5 Transconductance Amplifiers—Series-Series Feedback 616
11.4 Unified Approach to Feedback Amplifier Gain Calculation 616

11.4.1 Closed-Loop Gain Analysis 617
11.4.2 Resistance Calculation Using Blackman'S Theorem 617
11.5 Series-Shunt Feedback–Voltage Amplifiers 617
11.5.1 Closed-Loop Gain Calculation 618
11.5.2 Input Resistance Calculation 618
11.5.3 Output Resistance Calculation 619
11.5.4 Series-Shunt Feedback Amplifier Summary 620
11.6 Shunt-Shunt Feedback—Transresistance Amplifiers 624
11.6.1 Closed-Loop Gain Calculation 625
11.6.2 Input Resistance Calculation 625
11.6.3 Output Resistance Calculation 625
11.6.4 Shunt-Shunt Feedback Amplifier Summary 626
11.7 Series-Series Feedback—Transconductance Amplifiers 629
11.7.1 Closed-Loop Gain Calculation 630
11.7.2 Input Resistance Calculation 630
11.7.3 Output Resistance Calculation 631
11.7.4 Series-Series Feedback Amplifier Summary 631
11.8 Shunt-Series Feedback—Current Amplifiers 633
11.8.1 Closed-Loop Gain Calculation 634
11.8.2 Input Resistance Calculation 635
11.8.3 Output Resistance Calculation 635
11.8.4 Series-Series Feedback Amplifier Summary 635
11.9 Finding the Loop Gain Using Successive Voltage and Current Injection 638
11.9.1 Simplifications 641
11.10 Distortion Reduction Through the Use of Feedback 641
11.11 DC Error Sources and Output Range Limitations 642
11.11.1 Input-Offset Voltage 643
11.11.2 Offset-Voltage Adjustment 644
11.11.3 Input-Bias and Offset Currents 645
11.11.4 Output Voltage and Current Limits 647
11.12 Common-Mode Rejection and Input Resistance 650
11.12.1 Finite Common-Mode Rejection Ratio 650
11.12.2 Why Is CMRR Important? 651
11.12.3 Voltage-Follower Gain Error Due to CMRR 654
11.12.4 Common-Mode Input Resistance 656
11.12.5 An Alternate Interpretation of CMRR 657
11.12.6 Power Supply Rejection Ratio 657
11.13 Frequency Response and Bandwidth of Operational Amplifiers 659
11.13.1 Frequency Response of the Noninverting Amplifier 661
11.13.2 Inverting Amplifier Frequency Response 664
11.13.3 Using Feedback to Control Frequency Response 666
11.13.4 Large-Signal Limitations—Slew Rate and Full-Power Bandwidth 668
11.13.5 Macro Model for Operational Amplifier Frequency Response 669
11.13.6 Complete Op Amp Macro Models in SPICE 670
11.13.7 Examples of Commercial General-Purpose Operational Amplifiers 670
11.14 Stability of Feedback Amplifiers 671
11.14.1 The Nyquist Plot 671
11.14.2 First-Order Systems 672
11.14.3 Second-Order Systems and Phase Margin 673
11.14.4 Step Response and Phase Margin 674
11.14.5 Third-Order Systems and Gain Margin 677
11.14.6 Determining Stability from the Bode Plot 678
*Summary 682*
*Key Terms 684*
*References 684*
*Problems 685*

**CHAPTER 12**
**OPERATIONAL AMPLIFIER APPLICATIONS 697**

12.1 Cascaded Amplifiers 698
12.1.1 Two-Port Representations 698
12.1.2 Amplifier Terminology Review 700
12.1.3 Frequency Response of Cascaded Amplifiers 703
12.2 The Instrumentation Amplifier 711
12.3 Active Filters 714
12.3.1 Low-Pass Filter 714
12.3.2 A High-Pass Filter with Gain 718
12.3.3 Band-Pass Filter 720
12.3.4 The Tow-Thomas Biquad 722
12.3.5 Sensitivity 726
12.3.6 Magnitude and Frequency Scaling 727

12.4 Switched-Capacitor Circuits 728
12.4.1 A Switched-Capacitor Integrator 728
12.4.2 Noninverting SC Integrator 730
12.4.3 Switched-Capacitor Filters 732
12.5 Digital-to-Analog Conversion 733
12.5.1 D/A Converter Fundamentals 733
12.5.2 D/A Converter Errors 734
12.5.3 Digital-to-Analog Converter Circuits 737
12.6 Analog-to-Digital Conversion 740
12.6.1 A/D Converter Fundamentals 741
12.6.2 Analog-to-Digital Converter Errors 742
12.6.3 Basic A/D Conversion Techniques 743
12.7 Oscillators 754
12.7.1 The Barkhausen Criteria for Oscillation 754
12.7.2 Oscillators Employing Frequency-Selective *RC* Networks 755
12.8 Nonlinear Circuit Applications 760
12.8.1 A Precision Half-Wave Rectifier 760
12.8.2 Nonsaturating Precision-Rectifier Circuit 761
12.9 Circuits Using Positive Feedback 763
12.9.1 The Comparator and Schmitt Trigger 763
12.9.2 The Astable Multivibrator 765
12.9.3 The Monostable Multivibrator or One Shot 766
*Summary 770*
*Key Terms 772*
*Additional Reading 773*
*Problems 773*

**CHAPTER 13**

**SMALL-SIGNAL MODELING AND LINEAR AMPLIFICATION 786**

13.1 The Transistor as an Amplifier 787
13.1.1 The BJT Amplifier 788
13.1.2 The MOSFET Amplifier 789
13.2 Coupling and Bypass Capacitors 790
13.3 Circuit Analysis Using dc and ac Equivalent Circuits 792
13.3.1 Menu for dc and ac Analysis 792
13.4 Introduction to Small-Signal Modeling 796
13.4.1 Graphical Interpretation of the Small-Signal Behavior of the Diode 796
13.4.2 Small-Signal Modeling of the Diode 797
13.5 Small-Signal Models for Bipolar Junction Transistors 799
13.5.1 The Hybrid-Pi Model 801
13.5.2 Graphical Interpretation of the Transconductance 802
13.5.3 Small-Signal Current Gain 802
13.5.4 The Intrinsic Voltage Gain of the BJT 803
13.5.5 Equivalent Forms of the Small-Signal Model 804
13.5.6 Simplified Hybrid Pi Model 805
13.5.7 Definition of a Small Signal for the Bipolar Transistor 805
13.5.8 Small-Signal Model for the *pnp* Transistor 807
13.5.9 ac Analysis Versus Transient Analysis in SPICE 807
13.6 The Common-Emitter (C-E) Amplifier 808
13.6.1 Terminal Voltage Gain 809
13.6.2 Input Resistance 809
13.6.3 Signal Source Voltage Gain 810
13.7 Important Limits and Model Simplifications 810
13.7.1 A Design Guide for the Common-Emitter Amplifier 810
13.7.2 Upper Bound on the Common-Emitter Gain 812
13.7.3 Small-Signal Limit for the Common-emitter Amplifier 812
13.8 Small-Signal Models for Field-Effect Transistors 815
13.8.1 Small-Signal Model for the MOSFET 815
13.8.2 Intrinsic Voltage Gain of the MOSFET 817
13.8.3 Definition of Small-Signal Operation for the MOSFET 817
13.8.4 Body Effect in the Four-Terminal MOSFET 818
13.8.5 Small-Signal Model for the PMOS Transistor 819
13.8.6 Small-Signal Model for the Junction Field-Effect Transistor 820
13.9 Summary and Comparison of the Small-Signal Models of the BJT and FET 821
13.10 The Common-Source Amplifier 824
13.10.1 Common-Source Terminal Voltage Gain 825
13.10.2 Signal Source Voltage Gain for the Common-Source Amplifier 825
13.10.3 A Design Guide for the Common-Source Amplifier 826
13.10.4 Small-Signal Limit for the Common-Source Amplifier 827

13.10.5 Input Resistances of the Common-Emitter and Common-Source Amplifiers 829
13.10.6 Common-Emitter and Common-Source Output Resistances 832
13.10.7 Comparison of the Three Amplifier Resistances 838
13.11 Common-Emitter and Common-Source Amplifier Summary 838
13.11.1 Guidelines for Neglecting the Transistor Output Resistance 839
13.12 Amplifier Power and Signal Range 839
13.12.1 Power Dissipation 839
13.12.2 Signal Range 840
*Summary 843*
*Key Terms 844*
*Problems 845*

**CHAPTER 14**
**SINGLE-TRANSISTOR AMPLIFIERS 857**

14.1 Amplifier Classification 858
14.1.1 Signal Injection and Extraction—The BJT 858
14.1.2 Signal Injection and Extraction—The FET 859
14.1.3 Common-Emitter (C-E) and Common-Source (C-S) Amplifiers 860
14.1.4 Common-Collector (C-C) and Common-Drain (C-D) Topologies 861
14.1.5 Common-Base (C-B) and Common-Gate (C-G) Amplifiers 863
14.1.6 Small-Signal Model Review 864
14.2 Inverting Amplifiers—Common-Emitter and Common-Source Circuits 864
14.2.1 The Common-Emitter (C-E) Amplifier 864
14.2.2 Common-Emitter Example Comparison 877
14.2.3 The Common-Source Amplifier 877
14.2.4 Small-Signal Limit for the Common-Source Amplifier 880
14.2.5 Common-Emitter and Common-Source Amplifier Characteristics 884
14.2.6 C-E/C-S Amplifier Summary 885
14.2.7 Equivalent Transistor Representation of the Generalized C-E/C-S Transistor 885
14.3 Follower Circuits—Common-Collector and Common-Drain Amplifiers 886
14.3.1 Terminal Voltage Gain 886
14.3.2 Input Resistance 887
14.3.3 Signal Source Voltage Gain 888
14.3.4 Follower Signal Range 888
14.3.5 Follower Output Resistance 889
14.3.6 Current Gain 890
14.3.7 C-C/C-D Amplifier Summary 890
14.4 Noninverting Amplifiers—Common-Base and Common-Gate Circuits 894
14.4.1 Terminal Voltage Gain and Input Resistance 895
14.4.2 Signal Source Voltage Gain 896
14.4.3 Input Signal Range 897
14.4.4 Resistance at the Collector and Drain Terminals 897
14.4.5 Current Gain 898
14.4.6 Overall Input and Output Resistances for the Noninverting Amplifiers 899
14.4.7 C-B/C-G Amplifier Summary 902
14.5 Amplifier Prototype Review and Comparison 903
14.5.1 The BJT Amplifiers 903
14.5.2 The FET Amplifiers 905
14.6 Common-Source Amplifiers Using MOS Inverters 907
14.6.1 Voltage Gain Estimate 908
14.6.2 Detailed Analysis 909
14.6.3 Alternative Loads 910
14.6.4 Input and Output Resistances 911
14.7 Coupling and Bypass Capacitor Design 914
14.7.1 Common-Emitter and Common-Source Amplifiers 914
14.7.2 Common-Collector and Common-Drain Amplifiers 919
14.7.3 Common-Base and Common-Gate Amplifiers 921
14.7.4 Setting Lower Cutoff Frequency $f_L$ 924
14.8 Amplifier Design Examples 925
14.8.1 Monte Carlo Evaluation of the Common-Base Amplifier Design 934
14.9 Multistage ac-Coupled Amplifiers 939
14.9.1 A Three-Stage ac-Coupled Amplifier 939
14.9.2 Voltage Gain 941
14.9.3 Input Resistance 943
14.9.4 Signal Source Voltage Gain 943
14.9.5 Output Resistance 943
14.9.6 Current and Power Gain 944

14.9.7 Input Signal Range 945
14.9.8 Estimating the Lower Cutoff Frequency of the Multistage Amplifier 948
*Summary 950*
*Key Terms 951*
*Additional Reading 952*
*Problems 952*

CHAPTER 15
**DIFFERENTIAL AMPLIFIERS AND OPERATIONAL AMPLIFIER DESIGN 968**

15.1 Differential Amplifiers 969
15.1.1 Bipolar and MOS Differential Amplifiers 969
15.1.2 dc Analysis of the Bipolar Differential Amplifier 970
15.1.3 Transfer Characteristic for the Bipolar Differential Amplifier 972
15.1.4 ac Analysis of the Bipolar Differential Amplifier 973
15.1.5 Differential-Mode Gain and Input and Output Resistances 974
15.1.6 Common-Mode Gain and Input Resistance 976
15.1.7 Common-Mode Rejection Ratio (CMRR) 978
15.1.8 Analysis Using Differential- and Common-Mode Half-Circuits 979
15.1.9 Biasing with Electronic Current Sources 982
15.1.10 Modeling the Electronic Current Source in SPICE 983
15.1.11 dc Analysis of the MOSFET Differential Amplifier 983
15.1.12 Differential-Mode Input Signals 985
15.1.13 Small-Signal Transfer Characteristic for the MOS Differential Amplifier 986
15.1.14 Common-Mode Input Signals 986
15.1.15 Two-Port Model for Differential Pairs 987
15.2 Evolution to Basic Operational Amplifiers 991
15.2.1 A Two-Stage Prototype for an Operational Amplifier 992
15.2.2 Improving the Op Amp Voltage Gain 997
15.2.3 Output Resistance Reduction 998
15.2.4 A CMOS Operational Amplifier Prototype 1002
15.2.5 BiCMOS Amplifiers 1004
15.2.6 All Transistor Implementations 1004
15.3 Output Stages 1006
15.3.1 The Source Follower—A Class-A Output Stage 1006
15.3.2 Efficiency of Class-A Amplifiers 1007
15.3.3 Class-B Push-Pull Output Stage 1008
15.3.4 Class-AB Amplifiers 1010
15.3.5 Class-AB Output Stages for Operational Amplifiers 1011
15.3.6 Short-Circuit Protection 1011
15.3.7 Transformer Coupling 1013
15.4 Electronic Current Sources 1016
15.4.1 Single-Transistor Current Sources 1017
15.4.2 Figure of Merit for Current Sources 1017
15.4.3 Higher Output Resistance Sources 1018
15.4.4 Current Source Design Examples 1018
*Summary 1027*
*Key Terms 1028*
*References 1029*
*Additional Reading 1029*
*Problems 1029*

CHAPTER 16
**ANALOG INTEGRATED CIRCUIT DESIGN TECHNIQUES 1046**

16.1 Circuit Element Matching 1047
16.2 Current Mirrors 1049
16.2.1 dc Analysis of the MOS Transistor Current Mirror 1049
16.2.2 Changing the MOS Mirror Ratio 1051
16.2.3 dc Analysis of the Bipolar Transistor Current Mirror 1052
16.2.4 Altering the BJT Current Mirror Ratio 1054
16.2.5 Multiple Current Sources 1055
16.2.6 Buffered Current Mirror 1056
16.2.7 Output Resistance of the Current Mirrors 1057
16.2.8 Two-Port Model for the Current Mirror 1058
16.2.9 The Widlar Current Source 1060
16.2.10 The MOS Version of the Widlar Source 1063

16.3 High-Output-Resistance Current Mirrors 1063
16.3.1 The Wilson Current Sources 1064
16.3.2 Output Resistance of the Wilson Source 1065
16.3.3 Cascode Current Sources 1066
16.3.4 Output Resistance of the Cascode Sources 1067
16.3.5 Regulated Cascode Current Source 1068
16.3.6 Current Mirror Summary 1069
16.4 Reference Current Generation 1072
16.5 Supply-Independent Biasing 1073
16.5.1 A $V_{BE}$-Based Reference 1073
16.5.2 The Widlar Source 1073
16.5.3 Power-Supply-Independent Bias Cell 1074
16.5.4 A Supply-Independent MOS Reference Cell 1075
16.6 The Bandgap Reference 1077
16.7 The Current Mirror As an Active Load 1081
16.7.1 CMOS Differential Amplifier with Active Load 1081
16.7.2 Bipolar Differential Amplifier with Active Load 1088
16.8 Active Loads in Operational Amplifiers 1092
16.8.1 CMOS Op Amp Voltage Gain 1092
16.8.2 dc Design Considerations 1093
16.8.3 Bipolar Operational Amplifiers 1095
16.8.4 Input Stage Breakdown 1096
16.9 The μA741 Operational Amplifier 1097
16.9.1 Overall Circuit Operation 1097
16.9.2 Bias Circuitry 1098
16.9.3 dc Analysis of the 741 Input Stage 1099
16.9.4 ac Analysis of the 741 Input Stage 1102
16.9.5 Voltage Gain of the Complete Amplifier 1103
16.9.6 The 741 Output Stage 1107
16.9.7 Output Resistance 1109
16.9.8 Short Circuit Protection 1109
16.9.9 Summary of the μA741 Operational Amplifier Characteristics 1109
16.10 The Gilbert Analog Multiplier 1110
*Summary 1112*
*Key Terms 1113*
*References 1114*
*Problems 1114*

**CHAPTER 17**

**AMPLIFIER FREQUENCY RESPONSE 1128**

17.1 Amplifier Frequency Response 1129
17.1.1 Low-Frequency Response 1130
17.1.2 Estimating $\omega_L$ in the Absence of a Dominant Pole 1130
17.1.3 High-Frequency Response 1133
17.1.4 Estimating $\omega_H$ in the Absence of a Dominant Pole 1133
17.2 Direct Determination of the Low-Frequency Poles and Zeros—The Common-Source Amplifier 1134
17.3 Estimation of $\omega_L$ Using the Short-Circuit Time-Constant Method 1139
17.3.1 Estimate of $\omega_L$ for the Common-Emitter Amplifier 1140
17.3.2 Estimate of $\omega_L$ for the Common-Source Amplifier 1144
17.3.3 Estimate of $\omega_L$ for the Common-Base Amplifier 1145
17.3.4 Estimate of $\omega_L$ for the Common-Gate Amplifier 1146
17.3.5 Estimate of $\omega_L$ for the Common-Collector Amplifier 1147
17.3.6 Estimate of $\omega_L$ for the Common-Drain Amplifier 1147
17.4 Transistor Models at High Frequencies 1148
17.4.1 Frequency-Dependent Hybrid-Pi Model for the Bipolar Transistor 1148
17.4.2 Modeling $C_\pi$ and $C_\mu$ in SPICE 1149
17.4.3 Unity-Gain Frequency $f_T$ 1149
17.4.4 High-Frequency Model for the FET 1152
17.4.5 Modeling $C_{GS}$ and $C_{GD}$ in SPICE 1153
17.4.6 Channel Length Dependence of $f_T$ 1153
17.4.7 Limitations of the High-Frequency Models 1155
17.5 Base Resistance in the Hybrid-Pi Model 1155
17.5.1 Effect of Base Resistance on Midband Amplifiers 1156
17.6 High-Frequency Common-Emitter and Common-Source Amplifier Analysis 1158
17.6.1 The Miller Effect 1159
17.6.2 Common-Emitter and Common-Source Amplifier High-Frequency Response 1160
17.6.3 Direct Analysis of the Common-Emitter Transfer Characteristic 1162

17.6.4 Poles of the Common-Emitter Amplifier 1163
17.6.5 Dominant Pole for the Common-Source Amplifier 1166
17.6.6 Estimation of $\omega_H$ Using the Open-Circuit Time-Constant Method 1167
17.6.7 Common-Source Amplifier with Source Degeneration Resistance 1170
17.6.8 Poles of the Common-Emitter with Emitter Degeneration Resistance 1172
17.7 Common-Base and Common-Gate Amplifier High-Frequency Response 1174
17.8 Common-Collector and Common-Drain Amplifier High-Frequency Response 1177
17.9 Single-Stage Amplifier High-Frequency Response Summary 1179
17.9.1 Amplifier Gain-Bandwidth Limitations 1180
17.10 Frequency Response of Multistage Amplifiers 1181
17.10.1 Differential Amplifier 1181
17.10.2 The Common-Collector/Common-Base Cascade 1182
17.10.3 High-Frequency Response of the Cascode Amplifier 1184
17.10.4 Cutoff Frequency for the Current Mirror 1185
17.10.5 Three-Stage Amplifier Example 1187
17.11 Introduction to Radio Frequency Circuits 1193
17.11.1 Radio Frequency Amplifiers 1194
17.11.2 The Shunt-Peaked Amplifier 1194
17.11.3 Single-Tuned Amplifier 1197
17.11.4 Use of a Tapped Inductor—The Auto Transformer 1199
17.11.5 Multiple Tuned Circuits—Synchronous and Stagger Tuning 1201
17.11.6 Common-Source Amplifier with Inductive Degeneration 1202
17.12 Mixers and Balanced Modulators 1205
17.12.1 Introduction to Mixer Operation 1205
17.12.2 A Single-Balanced Mixer 1206
17.12.3 The Differential Pair as a Single-Balanced Mixer 1207
17.12.4 A Double-Balanced Mixer 1208
17.12.5 The Gilbert Multiplier as a Double-Balanced Mixer/Modulator 1210
*Summary 1213*
*Key Terms 1215*
*Reference 1215*
*Problems 1215*

CHAPTER 18
**TRANSISTOR FEEDBACK AMPLIFIERS AND OSCILLATORS 1228**

18.1 Basic Feedback System Review 1229
18.1.1 Closed-Loop Gain 1229
18.1.2 Closed-Loop Impedances 1230
18.1.3 Feedback Effects 1230
18.2 Feedback Amplifier Analysis at Midband 1232
18.3 Feedback Amplifier Circuit Examples 1234
18.3.1 Series-Shunt Feedback—Voltage Amplifiers 1234
18.3.2 Differential Input Series-Shunt Voltage Amplifier 1239
18.3.3 Shunt-Shunt Feedback—Transresistance Amplifiers 1242
18.3.4 Series-Series Feedback—Transconductance Amplifiers 1248
18.3.5 Shunt-Series Feedback—Current Amplifiers 1251
18.4 Review of Feedback Amplifier Stability 1254
18.4.1 Closed-Loop Response of the Uncompensated Amplifier 1254
18.4.2 Phase Margin 1256
18.4.3 Higher-Order Effects 1259
18.4.4 Response of the Compensated Amplifier 1260
18.4.5 Small-Signal Limitations 1262
18.5 Single-Pole Operational Amplifier Compensation 1262
18.5.1 Three-Stage Op Amp Analysis 1263
18.5.2 Transmission Zeros in FET Op Amps 1265
18.5.3 Bipolar Amplifier Compensation 1266
18.5.4 Slew Rate of the Operational Amplifier 1266
18.5.5 Relationships Between Slew Rate and Gain-Bandwidth Product 1268
18.6 High-Frequency Oscillators 1277
18.6.1 The Colpitts Oscillator 1278
18.6.2 The Hartley Oscillator 1279
18.6.3 Amplitude Stabilization in *LC* Oscillators 1280
18.6.4 Negative Resistance in Oscillators 1280

18.6.5 Negative $G_M$ Oscillator 1281
18.6.6 Crystal Oscillators 1283
*Summary 1287*
*Key Terms 1289*
*References 1289*
*Problems 1289*

## APPENDIXES

A Standard Discrete Component Values 1300
B Solid-State Device Models and SPICE Simulation Parameters 1303
C Two-Port Review 1310

Index 1313