

CONTENTS

Preface xx
Chapter-by-Chapter Summary xxv

PART ONE **SOLID-STATE ELECTRONICS AND DEVICES 1**

CHAPTER 1 INTRODUCTION TO ELECTRONICS 3

- 1.1 A Brief History of Electronics: From Vacuum Tubes to Giga-Scale Integration 5
- 1.2 Classification of Electronic Signals 8
 - 1.2.1 Digital Signals 9
 - 1.2.2 Analog Signals 9
 - 1.2.3 A/D and D/A Converters—Bridging the Analog and Digital Domains 10
- 1.3 Notational Conventions 12
- 1.4 Problem-Solving Approach 13
- 1.5 Important Concepts from Circuit Theory 15
 - 1.5.1 Voltage and Current Division 15
 - 1.5.2 Thévenin and Norton Circuit Representations 16
- 1.6 Frequency Spectrum of Electronic Signals 21
- 1.7 Amplifiers 22
 - 1.7.1 Ideal Operational Amplifiers 23
 - 1.7.2 Amplifier Frequency Response 25
- 1.8 Element Variations in Circuit Design 26
 - 1.8.1 Mathematical Modeling of Tolerances 26
 - 1.8.2 Worst-Case Analysis 27
 - 1.8.3 Monte Carlo Analysis 29
 - 1.8.4 Temperature Coefficients 32
- 1.9 Numeric Precision 34
 - Summary* 34
 - Key Terms* 35
 - References* 36
 - Additional Reading* 36
 - Problems* 36

CHAPTER 2 SOLID-STATE ELECTRONICS 41

- 2.1 Solid-State Electronic Materials 43
- 2.2 Covalent Bond Model 44
- 2.3 Drift Currents and Mobility in Semiconductors 47
 - 2.3.1 Drift Currents 47
 - 2.3.2 Mobility 48
 - 2.3.3 Velocity Saturation 48
- 2.4 Resistivity of Intrinsic Silicon 49
- 2.5 Impurities in Semiconductors 50
 - 2.5.1 Donor Impurities in Silicon 51
 - 2.5.2 Acceptor Impurities in Silicon 51
- 2.6 Electron and Hole Concentrations in Doped Semiconductors 51
 - 2.6.1 *n*-Type Material ($N_D > N_A$) 52
 - 2.6.2 *p*-Type Material ($N_A > N_D$) 53
- 2.7 Mobility and Resistivity in Doped Semiconductors 54
- 2.8 Diffusion Currents 58
- 2.9 Total Current 59
- 2.10 Energy Band Model 60
 - 2.10.1 Electron—Hole Pair Generation in an Intrinsic Semiconductor 60
 - 2.10.2 Energy Band Model for a Doped Semiconductor 61
 - 2.10.3 Compensated Semiconductors 61
- 2.11 Overview of Integrated Circuit Fabrication 63
 - Summary* 66
 - Key Terms* 67
 - Reference* 68
 - Additional Reading* 68
 - Problems* 68

CHAPTER 3 SOLID-STATE DIODES AND DIODE CIRCUITS 72

- 3.1 The *pn* Junction Diode 73
 - 3.1.1 *pn* Junction Electrostatics 73
 - 3.1.2 Internal Diode Currents 77
- 3.2 The *i-v* Characteristics of the Diode 78

3.3	The Diode Equation: A Mathematical Model for the Diode	80	3.15	Full-Wave Bridge Rectification	123
3.4	Diode Characteristics under Reverse, Zero, and Forward Bias	83	3.16	Rectifier Comparison and Design Tradeoffs	124
3.4.1	Reverse Bias	83	3.17	Dynamic Switching Behavior of the Diode	128
3.4.2	Zero Bias	83	3.18	Photo Diodes, Solar Cells, and Light-Emitting Diodes	129
3.4.3	Forward Bias	84	3.18.1	Photo Diodes and Photodetectors	129
3.5	Diode Temperature Coefficient	86	3.18.2	Power Generation from Solar Cells	130
3.6	Diodes under Reverse Bias	86	3.18.3	Light-Emitting Diodes (LEDs)	131
3.6.1	Saturation Current in Real Diodes	87		<i>Summary</i>	132
3.6.2	Reverse Breakdown	89		<i>Key Terms</i>	133
3.6.3	Diode Model for the Breakdown Region	90		<i>Reference</i>	134
3.7	<i>pn</i> Junction Capacitance	90		<i>Additional Reading</i>	134
3.7.1	Reverse Bias	90		<i>Problems</i>	134
3.7.2	Forward Bias	91			
3.8	Schottky Barrier Diode	93			
3.9	Diode SPICE Model and Layout	93			
3.9.1	Diode Layout	94			
3.10	Diode Circuit Analysis	95	4.1	Characteristics of the MOS Capacitor	145
3.10.1	Load-Line Analysis	96	4.1.1	Accumulation Region	146
3.10.2	Analysis Using the Mathematical Model for the Diode	97	4.1.2	Depletion Region	147
3.10.3	The Ideal Diode Model	101	4.1.3	Inversion Region	147
3.10.4	Constant Voltage Drop Model	103	4.2	The NMOS Transistor	147
3.10.5	Model Comparison and Discussion	104	4.2.1	Qualitative <i>i-v</i> Behavior of the NMOS Transistor	148
3.11	Multiple-Diode Circuits	105	4.2.2	Triode Region Characteristics of the NMOS Transistor	149
3.12	Analysis of Diodes Operating in the Breakdown Region	108	4.2.3	On Resistance	152
3.12.1	Load-Line Analysis	108	4.2.4	Transconductance	153
3.12.2	Analysis with the Piecewise Linear Model	108	4.2.5	Saturation of the <i>i-v</i> Characteristics	154
3.12.3	Voltage Regulation	109	4.2.6	Mathematical Model in the Saturation (Pinch-Off) Region	155
3.12.4	Analysis Including Zener Resistance	110	4.2.7	Transconductance in Saturation	156
3.12.5	Line and Load Regulation	111	4.2.8	Channel-Length Modulation	156
3.13	Half-Wave Rectifier Circuits	112	4.2.9	Transfer Characteristics and Depletion-Mode MOSFETs	157
3.13.1	Half-Wave Rectifier with Resistor Load	112	4.2.10	Body Effect or Substrate Sensitivity	159
3.13.2	Rectifier Filter Capacitor	113	4.3	PMOS Transistors	160
3.13.3	Half-Wave Rectifier with <i>RC</i> Load	114	4.4	MOSFET Circuit Symbols	162
3.13.4	Ripple Voltage and Conduction Interval	115	4.5	Capacitances in MOS Transistors	165
3.13.5	Diode Current	117	4.5.1	NMOS Transistor Capacitances in the Triode Region	165
3.13.6	Surge Current	119	4.5.2	Capacitances in the Saturation Region	166
3.13.7	Peak-Inverse-Voltage (PIV) Rating	119	4.5.3	Capacitances in Cutoff	166
3.13.8	Diode Power Dissipation	119	4.6	MOSFET Modeling in SPICE	167
3.13.9	Half-Wave Rectifier with Negative Output Voltage	120	4.7	MOS Transistor Scaling	168
3.14	Full-Wave Rectifier Circuits	122	4.7.1	Drain Current	169
3.14.1	Full-Wave Rectifier with Negative Output Voltage	123	4.7.2	Gate Capacitance	169
			4.7.3	Circuit and Power Densities	169

4.7.4	Power-Delay Product 170	5.3	The <i>pnp</i> Transistor 223
4.7.5	Cutoff Frequency 170	5.4	Equivalent Circuit Representations for the Transport Models 225
4.7.6	High Field Limitations 171	5.5	The <i>i-v</i> Characteristics of the Bipolar Transistor 226
4.7.7	The Unified MOS Transistor Model Including High Field Limitations 172	5.5.1	Output Characteristics 226
4.7.8	Subthreshold Conduction 173	5.5.2	Transfer Characteristics 227
4.8	MOS Transistor Fabrication and Layout Design Rules 174	5.6	The Operating Regions of the Bipolar Transistor 227
4.8.1	Minimum Feature Size and Alignment Tolerance 174	5.7	Transport Model Simplifications 228
4.8.2	MOS Transistor Layout 174	5.7.1	Simplified Model for the Cutoff Region 229
4.9	Biasing the NMOS Field-Effect Transistor 178	5.7.2	Model Simplifications for the Forward-Active Region 231
4.9.1	Why Do We Need Bias? 178	5.7.3	Diodes in Bipolar Integrated Circuits 237
4.9.2	Four-Resistor Biasing 180	5.7.4	Simplified Model for the Reverse-Active Region 238
4.9.3	Constant Gate-Source Voltage Bias 184	5.7.5	Modeling Operation in the Saturation Region 240
4.9.4	Graphical Analysis for the Q-Point 184	5.8	Nonideal Behavior of the Bipolar Transistor 243
4.9.5	Analysis Including Body Effect 184	5.8.1	Junction Breakdown Voltages 244
4.9.6	Analysis Using the Unified Model 187	5.8.2	Minority-Carrier Transport in the Base Region 244
4.10	Biasing the PMOS Field-Effect Transistor 188	5.8.3	Base Transit Time 245
4.11	The Junction Field-Effect Transistor (JFET) 190	5.8.4	Diffusion Capacitance 247
	4.11.1 The JFET with Bias Applied 191	5.8.5	Frequency Dependence of the Common-Emitter Current Gain 248
	4.11.2 JFET Channel with Drain-Source Bias 193	5.8.6	The Early Effect and Early Voltage 248
	4.11.3 <i>n</i> -Channel JFET <i>i-v</i> Characteristics 193	5.8.7	Modeling the Early Effect 249
	4.11.4 The <i>p</i> -Channel JFET 195	5.8.8	Origin of the Early Effect 249
	4.11.5 Circuit Symbols and JFET Model Summary 195	5.9	Transconductance 250
	4.11.6 JFET Capacitances 196	5.10	Bipolar Technology and SPICE Model 251
4.12	JFET Modeling in Spice 196	5.10.1	Qualitative Description 251
4.13	Biasing the JFET and Depletion-Mode MOSFET 197	5.10.2	SPICE Model Equations 252
	<i>Summary</i> 200	5.10.3	High-Performance Bipolar Transistors 253
	<i>Key Terms</i> 202	5.11	Practical Bias Circuits for the BJT 254
	<i>References</i> 202	5.11.1	Four-Resistor Bias Network 256
	<i>Problems</i> 203	5.11.2	Design Objectives for the Four-Resistor Bias Network 258
		5.11.3	Iterative Analysis of the Four-Resistor Bias Circuit 262
		5.12	Tolerances in Bias Circuits 262
		5.12.1	Worst-Case Analysis 263
		5.12.2	Monte Carlo Analysis 265
			<i>Summary</i> 268
			<i>Key Terms</i> 270
			<i>References</i> 270
			<i>Problems</i> 271

CHAPTER 5

BIPOLAR JUNCTION TRANSISTORS 215

5.1	Physical Structure of the Bipolar Transistor 216
5.2	The Transport Model for the <i>npn</i> Transistor 217
5.2.1	Forward Characteristics 218
5.2.2	Reverse Characteristics 220
5.2.3	The Complete Transport Model Equations for Arbitrary Bias Conditions 221

PART TWO

DIGITAL ELECTRONICS 281

CHAPTER 6

INTRODUCTION TO DIGITAL ELECTRONICS 283

- 6.1 Ideal Logic Gates 285
- 6.2 Logic Level Definitions and Noise Margins 285
 - 6.2.1 Logic Voltage Levels 287
 - 6.2.2 Noise Margins 287
 - 6.2.3 Logic Gate Design Goals 288
- 6.3 Dynamic Response of Logic Gates 289
 - 6.3.1 Rise Time and Fall Time 289
 - 6.3.2 Propagation Delay 290
 - 6.3.3 Power-Delay Product 290
- 6.4 Review of Boolean Algebra 291
- 6.5 NMOS Logic Design 293
 - 6.5.1 NMOS Inverter with Resistive Load 294
 - 6.5.2 Design of the W/L Ratio of M_s 295
 - 6.5.3 Load Resistor Design 296
 - 6.5.4 Load-Line Visualization 296
 - 6.5.5 On-Resistance of the Switching Device 298
 - 6.5.6 Noise Margin Analysis 299
 - 6.5.7 Calculation of V_{IL} and V_{OH} 299
 - 6.5.8 Calculation of V_{IH} and V_{OL} 300
 - 6.5.9 Resistor Load Inverter Noise Margins 300
 - 6.5.10 Load Resistor Problems 301
- 6.6 Transistor Alternatives to the Load Resistor 302
 - 6.6.1 The NMOS Saturated Load Inverter 303
 - 6.6.2 NMOS Inverter with a Linear Load Device 311
 - 6.6.3 NMOS Inverter with a Depletion-Mode Load 312
- 6.7 NMOS Inverter Summary and Comparison 315
- 6.8 Impact of Velocity Saturation on Static Inverter Design 316
 - 6.8.1 Switching Transistor Design 316
 - 6.8.2 Load Transistor Design 316
 - 6.8.3 Velocity Saturation Impact Summary 317
- 6.9 NMOS NAND and NOR Gates 317
 - 6.9.1 NOR Gates 318
 - 6.9.2 NAND Gates 319
 - 6.9.3 NOR and NAND Gate Layouts in NMOS Depletion-Mode Technology 320
- 6.10 Complex NMOS Logic Design 321
- 6.11 Power Dissipation 326

- 6.11.1 Static Power Dissipation 326
- 6.11.2 Dynamic Power Dissipation 327
- 6.11.3 Power Scaling in MOS Logic Gates 328
- 6.12 Dynamic Behavior of MOS Logic Gates 329
 - 6.12.1 Capacitances in Logic Circuits 330
 - 6.12.2 Dynamic Response of the NMOS Inverter with a Resistive Load 331
 - 6.12.3 Comparison of NMOS Inverter Delays 336
 - 6.12.4 Impact of Velocity Saturation on Inverter Delays 337
 - 6.12.5 Scaling Based upon Reference Circuit Simulation 337
 - 6.12.6 Ring Oscillator Measurement of Intrinsic Gate Delay 338
 - 6.12.7 Unloaded Inverter Delay 338
- 6.13 PMOS Logic 341
 - 6.13.1 PMOS Inverters 341
 - 6.13.2 NOR and NAND Gates 343
 - Summary 344*
 - Key Terms 346*
 - References 347*
 - Additional Reading 347*
 - Problems 347*

CHAPTER 7

COMPLEMENTARY MOS (CMOS) LOGIC DESIGN 359

- 7.1 CMOS Inverter Technology 360
 - 7.1.1 CMOS Inverter Layout 362
- 7.2 Static Characteristics of the CMOS Inverter 362
 - 7.2.1 CMOS Voltage Transfer Characteristics 363
 - 7.2.2 Noise Margins for the CMOS Inverter 365
- 7.3 Dynamic Behavior of the CMOS Inverter 367
 - 7.3.1 Propagation Delay Estimate 367
 - 7.3.2 Rise and Fall Times 369
 - 7.3.3 Performance Scaling 369
 - 7.3.4 Impact of Velocity Saturation on CMOS Inverter Delays 371
 - 7.3.5 Delay of Cascaded Inverters 372
- 7.4 Power Dissipation and Power Delay Product in CMOS 373
 - 7.4.1 Static Power Dissipation 373
 - 7.4.2 Dynamic Power Dissipation 374
 - 7.4.3 Power-Delay Product 375
- 7.5 CMOS NOR and NAND Gates 377
 - 7.5.1 CMOS NOR Gate 377
 - 7.5.2 CMOS NAND Gates 380

7.6	Design of Complex Gates in CMOS	381
7.7	Minimum Size Gate Design and Performance	387
7.8	Cascade Buffers	389
7.8.1	Cascade Buffer Delay Model	389
7.8.2	Optimum Number of Stages	390
7.9	The CMOS Transmission Gate	392
7.10	Bistable Circuits	393
7.10.1	The Bistable Latch	393
7.10.2	RS Flip-Flop	396
7.10.3	The D-Latch Using Transmission Gates	397
7.10.4	A Master-Slave D Flip-Flop	397
7.11	CMOS Latchup	397
	Summary	402
	Key Terms	403
	References	404
	Problems	404

CHAPTER 8

MOS MEMORY CIRCUITS 414

8.1	Random-Access Memory (RAM)	415
8.1.1	Random-Access Memory (RAM) Architecture	415
8.1.2	A 256-Mb Memory Chip	416
8.2	Static Memory Cells	417
8.2.1	Memory Cell Isolation and Access—the 6-T Cell	417
8.2.2	The Read Operation	418
8.2.3	Writing Data into the 6-T Cell	422
8.3	Dynamic Memory Cells	424
8.3.1	The One-Transistor Cell	425
8.3.2	Data Storage in the 1-T Cell	425
8.3.3	Reading Data from the 1-T Cell	427
8.3.4	The Four-Transistor Cell	428
8.4	Sense Amplifiers	430
8.4.1	A Sense Amplifier for the 6-T Cell	430
8.4.2	A Sense Amplifier for the 1-T Cell	432
8.4.3	The Boosted Wordline Circuit	433
8.4.4	Clocked CMOS Sense Amplifiers	434
8.5	Address Decoders	436
8.5.1	NOR Decoder	436
8.5.2	NAND Decoder	436
8.5.3	Pass-Transistor Column Decoder	438
8.6	Read-Only Memory (ROM)	439
8.7	Flash Memory	442
8.7.1	Floating Gate Technology	442
8.7.2	NOR Circuit Implementations	445
8.7.3	NAND Implementations	445
	Summary	447
	Key Terms	448
	References	449
	Problems	449

CHAPTER 9		
BIPOLAR LOGIC CIRCUITS 455		
9.1	The Current Switch (Emitter-Coupled Pair)	456
9.1.1	Mathematical Model for Static Behavior of the Current Switch	456
9.1.2	Current Switch Analysis for $v_I > V_{REF}$	458
9.1.3	Current Switch Analysis for $v_I < V_{REF}$	459
9.2	The Emitter-Coupled Logic (ECL) Gate	459
9.2.1	ECL Gate with $v_I = V_H$	460
9.2.2	ECL Gate with $v_I = V_L$	461
9.2.3	Input Current of the ECL Gate	461
9.2.4	ECL Summary	461
9.3	Noise Margin Analysis for the ECL Gate	462
9.3.1	V_{IL} , V_{OH} , V_{IH} , and V_{OL}	462
9.3.2	Noise Margins	463
9.4	Current Source Implementation	464
9.5	The ECL OR-NOR Gate	466
9.6	The Emitter Follower	468
9.6.1	Emitter Follower with a Load Resistor	469
9.7	"Emitter Dotting" or "Wired-OR" Logic	471
9.7.1	Parallel Connection of Emitter-Follower Outputs	472
9.7.2	The Wired-OR Logic Function	472
9.8	ECL Power-Delay Characteristics	472
9.8.1	Power Dissipation	472
9.8.2	Gate Delay	474
9.8.3	Power-Delay Product	475
9.9	Positive ECL (PECL)	476
9.10	Current Mode Logic	476
9.10.1	CML Logic Gates	477
9.10.2	CML Logic Levels	478
9.10.3	V_{EE} Supply Voltage	478
9.10.4	Higher-Level CML	479
9.10.5	CML Power Reduction	480
9.10.6	Source-Coupled Fet Logic (SCFL)	480
9.11	The Saturating Bipolar Inverter	483
9.11.1	Static Inverter Characteristics	483
9.11.2	Saturation Voltage of the Bipolar Transistor	484
9.11.3	Load-Line Visualization	486
9.11.4	Switching Characteristics of the Saturated BJT	487
9.12	A Transistor-Transistor Logic (TTL)	490
9.12.1	TTL Inverter Analysis for $v_I = V_L$	490
9.12.2	Analysis for $v_I = V_H$	492
9.12.3	Power Consumption	493
9.12.4	TTL Propagation Delay and Power-Delay Product	493

9.12.5	TTL Voltage Transfer Characteristic and Noise Margins 494	10.9.1	The Inverting Amplifier 541
9.12.6	Fanout Limitations of Standard TTL 494	10.9.2	The Transresistance Amplifier—a Current-to-Voltage Converter 544
9.13	Logic Functions in TTL 494	10.9.3	The Noninverting Amplifier 546
9.13.1	Multi-Emitter Input Transistors 495	10.9.4	The Unity-Gain Buffer, or Voltage Follower 548
9.13.2	TTL NAND Gates 495	10.9.5	The Summing Amplifier 551
9.13.3	Input Clamping Diodes 496	10.9.6	The Difference Amplifier 553
9.14	Schottky-Clamped TTL 497	10.10	Frequency Dependent Feedback 555
9.15	Comparison of the Power-Delay Products of ECL and TTL 498	10.10.1	Bode Plots 556
9.16	BiCMOS Logic 498	10.10.2	The Low-Pass Amplifier 556
9.16.1	BiCMOS Buffers 499	10.10.3	The High-Pass Amplifier 559
9.16.2	BiNMOS Inverters 501	10.10.4	Band-Pass Amplifiers 562
9.16.3	BiCMOS Logic Gates 502	10.10.5	An Active Low-Pass Filter 565
	<i>Summary</i> 503	10.10.6	An Active High-Pass Filter 569
	<i>Key Terms</i> 504	10.10.7	The Integrator 570
	<i>References</i> 505	10.10.8	The Differentiator 573
	<i>Additional Reading</i> 505		<i>Summary</i> 574
	<i>Problems</i> 505		<i>Key Terms</i> 575
			<i>References</i> 576
			<i>Additional Reading</i> 576
			<i>Problems</i> 576

PART THREE

ANALOG ELECTRONICS 515

CHAPTER 10	
ANALOG SYSTEMS AND IDEAL OPERATIONAL AMPLIFIERS	517
10.1	An Example of an Analog Electronic System 518
10.2	Amplification 519
10.2.1	Voltage Gain 520
10.2.2	Current Gain 521
10.2.3	Power Gain 521
10.2.4	The Decibel Scale 522
10.3	Two-Port Models for Amplifiers 525
10.3.1	The <i>g</i> -Parameters 525
10.4	Mismatched Source and Load Resistances 529
10.5	Introduction to Operational Amplifiers 532
10.5.1	The Differential Amplifier 532
10.5.2	Differential Amplifier Voltage Transfer Characteristic 533
10.5.3	Voltage Gain 533
10.6	Distortion in Amplifiers 536
10.7	Differential Amplifier Model 537
10.8	Ideal Differential and Operational Amplifiers 539
10.8.1	Assumptions for Ideal Operational Amplifier Analysis 539
10.9	Analysis of Circuits Containing Ideal Operational Amplifiers 540

CHAPTER 11

NONIDEAL OPERATIONAL AMPLIFIERS AND FEEDBACK AMPLIFIER STABILITY 587

11.1	Classic Feedback Systems 588
11.1.1	Closed-Loop Gain Analysis 589
11.1.2	Gain Error 589
11.2	Analysis of Circuits Containing Nonideal Operational Amplifiers 590
11.2.1	Finite Open-Loop Gain 590
11.2.2	Nonzero Output Resistance 593
11.2.3	Finite Input Resistance 597
11.2.4	Summary of Nonideal Inverting and Noninverting Amplifiers 601
11.3	Series and Shunt Feedback Circuits 602
11.3.1	Feedback Amplifier Categories 602
11.3.2	Voltage Amplifiers—Series-Shunt Feedback 603
11.3.3	Transimpedance Amplifiers—Shunt-Shunt Feedback 603
11.3.4	Current Amplifiers—Shunt-Series Feedback 603
11.3.5	Transconductance Amplifiers—Series-Series Feedback 603
11.4	Unified Approach to Feedback Amplifier Gain Calculation 603
11.4.1	Closed-Loop Gain Analysis 604
11.4.2	Resistance Calculations Using Blackman's Theorem 604

11.5	Series-Shunt Feedback—Voltage Amplifiers 604	11.13	Frequency Response and Bandwidth of Operational Amplifiers 647
11.5.1	Closed-Loop Gain Calculation 605	11.13.1	Frequency Response of the Noninverting Amplifier 649
11.5.2	Input Resistance Calculations 605	11.13.2	Inverting Amplifier Frequency Response 652
11.5.3	Output Resistance Calculations 606	11.13.3	Using Feedback to Control Frequency Response 654
11.5.4	Series-Shunt Feedback Amplifier Summary 607	11.13.4	Large-Signal Limitations—Slew Rate and Full-Power Bandwidth 656
11.6	Shunt-Shunt Feedback—Transresistance Amplifiers 611	11.13.5	Macro Model for Operational Amplifier Frequency Response 657
11.6.1	Closed-Loop Gain Calculation 611	11.13.6	Complete Op Amp Macro Models in SPICE 658
11.6.2	Input Resistance Calculations 612	11.13.7	Examples of Commercial General-Purpose Operational Amplifiers 658
11.6.3	Output Resistance Calculations 612	11.14	Stability of Feedback Amplifiers 659
11.6.4	Shunt-Shunt Feedback Amplifier Summary 613	11.14.1	The Nyquist Plot 659
11.7	Series-Series Feedback—Transconductance Amplifiers 616	11.14.2	First-Order Systems 660
11.7.1	Closed-Loop Gain Calculation 617	11.14.3	Second-Order Systems and Phase Margin 661
11.7.2	Input Resistance Calculation 617	11.14.4	Step Response and Phase Margin 662
11.7.3	Output Resistance Calculation 618	11.14.5	Third-Order Systems and Gain Margin 665
11.7.4	Series-Series Feedback Amplifier Summary 618	11.14.6	Determining Stability from the Bode Plot 666
11.8	Shunt-Series Feedback—Current Amplifiers 620		<i>Summary</i> 670
11.8.1	Closed-Loop Gain Calculation 621		<i>Key Terms</i> 672
11.8.2	Input Resistance Calculation 621		<i>References</i> 672
11.8.3	Output Resistance Calculation 622		<i>Problems</i> 673
11.8.4	Series-Series Feedback Amplifier Summary 622		
11.9	Finding the Loop Gain Using Successive Voltage and Current Injection 625		
11.9.1	Simplifications 628		
11.10	Distortion Reduction through the Use of Feedback 628		
11.11	dc Error Sources and Output Range Limitations 629		
11.11.1	Input-Offset Voltage 629	12.1	Cascaded Amplifiers 686
11.11.2	Offset-Voltage Adjustment 631	12.1.1	Two-Port Representations 686
11.11.3	Input-Bias and Offset Currents 632	12.1.2	Amplifier Terminology Review 688
11.11.4	Output Voltage and Current Limits 634	12.1.3	Frequency Response of Cascaded Amplifiers 691
11.12	Common-Mode Rejection and Input Resistance 637	12.2	The Instrumentation Amplifier 699
11.12.1	Finite Common-Mode Rejection Ratio 637	12.3	Active Filters 702
11.12.2	Why Is CMRR Important? 638	12.3.1	Low-Pass Filter 702
11.12.3	Voltage-Follower Gain Error due to CMRR 641	12.3.2	A High-Pass Filter with Gain 706
11.12.4	Common-Mode Input Resistance 644	12.3.3	Band-Pass Filter 708
11.12.5	An Alternate Interpretation of CMRR 645	12.3.4	Sensitivity 710
11.12.6	Power Supply Rejection Ratio 645	12.3.5	Magnitude and Frequency Scaling 711

CHAPTER 12

OPERATIONAL AMPLIFIER APPLICATIONS 685

12.1	Cascaded Amplifiers 686
12.1.1	Two-Port Representations 686
12.1.2	Amplifier Terminology Review 688
12.1.3	Frequency Response of Cascaded Amplifiers 691
12.2	The Instrumentation Amplifier 699
12.3	Active Filters 702
12.3.1	Low-Pass Filter 702
12.3.2	A High-Pass Filter with Gain 706
12.3.3	Band-Pass Filter 708
12.3.4	Sensitivity 710
12.3.5	Magnitude and Frequency Scaling 711
12.4	Switched-Capacitor Circuits 712
12.4.1	A Switched-Capacitor Integrator 712

12.4.2	Noninverting SC Integrator	714	13.5.2	Graphical Interpretation of the Transconductance	786
12.4.3	Switched-Capacitor Filters	716	13.5.3	Small-Signal Current Gain	786
12.5	Digital-to-Analog Conversion	719	13.5.4	The Intrinsic Voltage Gain of the BJT	787
12.5.1	D/A Converter Fundamentals	719	13.5.5	Equivalent Forms of the Small-Signal Model	788
12.5.2	D/A Converter Errors	720	13.5.6	Simplified Hybrid Pi Model	789
12.5.3	Digital-to-Analog Converter Circuits	722	13.5.7	Definition of a Small Signal for the Bipolar Transistor	789
12.6	Analog-to-Digital Conversion	726	13.5.8	Small-Signal Model for the <i>pnp</i> Transistor	791
12.6.1	A/D Converter Fundamentals	727	13.5.9	ac Analysis versus Transient Analysis in SPICE	792
12.6.2	Analog-to-Digital Converter Errors	728	13.6	The Common-Emitter (C-E) Amplifier	792
12.6.3	Basic A/D Conversion Techniques	729	13.6.1	Terminal Voltage Gain	792
12.7	Oscillators	740	13.6.2	Input Resistance	794
12.7.1	The Barkhausen Criteria for Oscillation	740	13.6.3	Signal Source Voltage Gain	794
12.7.2	Oscillators Employing Frequency-Selective RC Networks	741	13.7	Important Limits and Model Simplifications	794
12.8	Nonlinear Circuit Applications	745	13.7.1	A Design Guide for the Common-Emitter Amplifier	795
12.8.1	A Precision Half-Wave Rectifier	745	13.7.2	Upper Bound on the Common-Emitter Gain	796
12.8.2	Nonsaturating Precision-Rectifier Circuit	746	13.7.3	Small-Signal Limit for the Common-Emitter Amplifier	796
12.9	Circuits Using Positive Feedback	748	13.8	Small-Signal Models for Field-Effect Transistors	799
12.9.1	The Comparator and Schmitt Trigger	748	13.8.1	Small-Signal Model for the MOSFET	799
12.9.2	The Astable Multivibrator	750	13.8.2	Intrinsic Voltage Gain of the MOSFET	801
12.9.3	The Monostable Multivibrator or One Shot	751	13.8.3	Definition of Small-Signal Operation for the MOSFET	802
	<i>Summary</i>	755	13.8.4	Body Effect in the Four-Terminal MOSFET	803
	<i>Key Terms</i>	757	13.8.5	Small-Signal Model for the PMOS Transistor	804
	<i>Additional Reading</i>	758	13.8.6	Small-Signal Model for the Junction Field-Effect Transistor	805
	<i>Problems</i>	758	13.9	Summary and Comparison of the Small-Signal Models of the BJT and FET	806
CHAPTER 13					
SMALL-SIGNAL MODELING AND LINEAR AMPLIFICATION 770					
13.1	The Transistor as an Amplifier	771	13.10	The Common-Source Amplifier	809
13.1.1	The BJT Amplifier	772	13.10.1	Common-Source Terminal Voltage Gain	810
13.1.2	The MOSFET Amplifier	773	13.10.2	Signal Source Voltage Gain for the Common-Source Amplifier	810
13.2	Coupling and Bypass Capacitors	774	13.10.3	A Design Guide for the Common-Source Amplifier	810
13.3	Circuit Analysis Using dc and ac Equivalent Circuits	776	13.10.4	Small-Signal Limit for the Common-Source Amplifier	811
13.3.1	Menu for dc and ac Analysis	776	13.10.5	Input Resistances of the Common-Emitter and Common-Source Amplifiers	813
13.4	Introduction to Small-Signal Modeling	780			
13.4.1	Graphical Interpretation of the Small-Signal Behavior of the Diode	780			
13.4.2	Small-Signal Modeling of the Diode	781			
13.5	Small-Signal Models for Bipolar Junction Transistors	783			
13.5.1	The Hybrid-Pi Model	785			

13.1	The Transistor as an Amplifier	771
13.1.1	The BJT Amplifier	772
13.1.2	The MOSFET Amplifier	773
13.2	Coupling and Bypass Capacitors	774
13.3	Circuit Analysis Using dc and ac Equivalent Circuits	776
13.3.1	Menu for dc and ac Analysis	776
13.4	Introduction to Small-Signal Modeling	780
13.4.1	Graphical Interpretation of the Small-Signal Behavior of the Diode	780
13.4.2	Small-Signal Modeling of the Diode	781
13.5	Small-Signal Models for Bipolar Junction Transistors	783
13.5.1	The Hybrid-Pi Model	785

13.10.6	Common-Emitter and Common-Source Output Resistances	816	14.3.3	Signal Source Voltage Gain	872
13.10.7	Comparison of the Three Amplifier Examples	822	14.3.4	Follower Signal Range	872
13.11	Common-Emitter and Common-Source Amplifier Summary	822	14.3.5	Follower Output Resistance	873
13.11.1	Guidelines for Neglecting the Transistor Output Resistance	823	14.3.6	Current Gain	874
13.12	Amplifier Power and Signal Range	823	14.3.7	C-C/C-D Amplifier Summary	874
13.12.1	Power Dissipation	823	14.4	Noninverting Amplifiers—Common-Base and Common-Gate Circuits	878
13.12.2	Signal Range Summary	824	14.4.1	Terminal Voltage Gain and Input Resistance	879
Key Terms	828	14.4.2	Signal Source Voltage Gain	880	
Problems	829	14.4.3	Input Signal Range	881	
CHAPTER 14					
SINGLE-TRANSISTOR AMPLIFIERS 841					
14.1	Amplifier Classification	842	14.4.4	Resistance at the Collector and Drain Terminals	881
14.1.1	Signal Injection and Extraction—the BJT	842	14.4.5	Current Gain	882
14.1.2	Signal Injection and Extraction—the FET	843	14.4.6	Overall Input and Output Resistances for the Noninverting Amplifiers	883
14.1.3	Common-Emitter (C-E) and Common-Source (C-S) Amplifiers	844	14.4.7	C-B/C-G Amplifier Summary	886
14.1.4	Common-Collector (C-C) and Common-Drain (C-D) Topologies	845	14.5	Amplifier Prototype Review and Comparison	887
14.1.5	Common-Base (C-B) and Common-Gate (C-G) Amplifiers	847	14.5.1	The BJT Amplifiers	887
14.1.6	Small-Signal Model Review	848	14.5.2	The FET Amplifiers	889
14.2	Inverting Amplifiers—Common-Emitter and Common-Source Circuits	848	14.6	Common-Source Amplifiers Using MOS Inverters	891
14.2.1	The Common-Emitter (C-E) Amplifier	848	14.6.1	Voltage Gain Estimate	892
14.2.2	Common-Emitter Example Comparison	861	14.6.2	Detailed Analysis	893
14.2.3	The Common-Source Amplifier	861	14.6.3	Alternative Loads	894
14.2.4	Small-Signal Limit for the Common-Source Amplifier	864	14.6.4	Input and Output Resistances	895
14.2.5	Common-Emitter and Common-Source Amplifier Characteristics	868	14.7	Coupling and Bypass Capacitor Design	898
14.2.6	C-E/C-S Amplifier Summary	869	14.7.1	Common-Emitter and Common-Source Amplifiers	898
14.2.7	Equivalent Transistor Representation of the Generalized C-E/C-S Transistor	869	14.7.2	Common-Collector and Common-Drain Amplifiers	903
14.3	Follower Circuits—Common-Collector and Common-Drain Amplifiers	870	14.7.3	Common-Base and Common-Gate Amplifiers	905
14.3.1	Terminal Voltage Gain	870	14.7.4	Setting Lower Cutoff Frequency f_L	908
14.3.2	Input Resistance	871	14.8	Amplifier Design Examples	909
14.9.1	A Three-Stage ac-Coupled Amplifier	923	14.8.1	Monte Carlo Evaluation of the Common-Base Amplifier Design	918
14.9.2	Voltage Gain	925	14.9	Multistage ac-Coupled Amplifiers	923
14.9.3	Input Resistance	927	14.9.1		
14.9.4	Signal Source Voltage Gain	927	14.9.2		
14.9.5	Output Resistance	927	14.9.3		
14.9.6	Current and Power Gain	928	14.9.4		
14.9.7	Input Signal Range	929	14.9.5		
14.9.8	Estimating the Lower Cutoff Frequency of the Multistage Amplifier	932	14.9.6		

Summary	934
Key Terms	935
Additional Reading	936
Problems	936

CHAPTER 15**DIFFERENTIAL AMPLIFIERS AND OPERATIONAL AMPLIFIER DESIGN 952**

15.1	Differential Amplifiers	953
15.1.1	Bipolar and MOS Differential Amplifiers	953
15.1.2	dc Analysis of the Bipolar Differential Amplifier	954
15.1.3	Transfer Characteristic for the Bipolar Differential Amplifier	956
15.1.4	ac Analysis of the Bipolar Differential Amplifier	957
15.1.5	Differential-Mode Gain and Input and Output Resistances	958
15.1.6	Common-Mode Gain and Input Resistance	960
15.1.7	Common-Mode Rejection Ratio (CMRR)	962
15.1.8	Analysis Using Differential- and Common-Mode Half-Circuits	963
15.1.9	Biasing with Electronic Current Sources	966
15.1.10	Modeling the Electronic Current Source in SPICE	967
15.1.11	dc Analysis of the MOSFET Differential Amplifier	967
15.1.12	Differential-Mode Input Signals	970
15.1.13	Small-Signal Transfer Characteristic for the MOS Differential Amplifier	971
15.1.14	Common-Mode Input Signals	971
15.1.15	Model for Differential Pairs	972
15.2	Evolution to Basic Operational Amplifiers	976
15.2.1	A Two-Stage Prototype for an Operational Amplifier	977
15.2.2	Improving the Op Amp Voltage Gain	982
15.2.3	Darlington Pairs	983
15.2.4	Output Resistance Reduction	984
15.2.5	A CMOS Operational Amplifier Prototype	988
15.2.6	BiCMOS Amplifiers	990
15.2.7	All Transistor Implementations	990
15.3	Output Stages	992
15.3.1	The Source Follower—a Class-A Output Stage	992

15.3.2	Efficiency of Class-A Amplifiers	993
15.3.3	Class-B Push-Pull Output Stage	994
15.3.4	Class-AB Amplifiers	996
15.3.5	Class-AB Output Stages for Operational Amplifiers	997
15.3.6	Short-Circuit Protection	997
15.3.7	Transformer Coupling	999
15.4	Electronic Current Sources	1002
15.4.1	Single-Transistor Current Sources	1003
15.4.2	Figure of Merit for Current Sources	1003
15.4.3	Higher Output Resistance Sources	1004
15.4.4	Current Source Design Examples	1005
	Summary	1013
	Key Terms	1014
	References	1015
	Additional Reading	1015
	Problems	1015

CHAPTER 16**ANALOG INTEGRATED CIRCUIT DESIGN TECHNIQUES 1031**

16.1	Circuit Element Matching	1032
16.2	Current Mirrors	1033
16.2.1	dc Analysis of the MOS Transistor Current Mirror	1034
16.2.2	Changing the MOS Mirror Ratio	1036
16.2.3	dc Analysis of the Bipolar Transistor Current Mirror	1037
16.2.4	Altering the BJT Current Mirror Ratio	1039
16.2.5	Multiple Current Sources	1040
16.2.6	Buffered Current Mirror	1041
16.2.7	Output Resistance of the Current Mirrors	1042
16.2.8	Two-Port Model for the Current Mirror	1043
16.2.9	The Widlar Current Source	1045
16.2.10	The MOS Version of the Widlar Source	1048
16.3	High-Output-Resistance Current Mirrors	1048
16.3.1	The Wilson Current Sources	1049
16.3.2	Output Resistance of the Wilson Source	1050
16.3.3	Cascode Current Sources	1051
16.3.4	Output Resistance of the Cascode Sources	1052

16.3.5	Regulated Cascode Current Source 1053	17.2	Direct Determination of the Low-Frequency Poles and Zeros—the Common-Source Amplifier 1119
16.3.6	Current Mirror Summary 1054	17.3	Estimation of ω_L Using the Short-Circuit Time-Constant Method 1124
16.4	Reference Current Generation 1057	17.3.1	Estimate of ω_L for the Common-Emitter Amplifier 1125
16.5	Supply-Independent Biasing 1058	17.3.2	Estimate of ω_L for the Common-Source Amplifier 1129
16.5.1	A V_{BE} -Based Reference 1058	17.3.3	Estimate of ω_L for the Common-Base Amplifier 1130
16.5.2	The Widlar Source 1058	17.3.4	Estimate of ω_L for the Common-Gate Amplifier 1131
16.5.3	Power-Supply-Independent Bias Cell 1059	17.3.5	Estimate of ω_L for the Common-Collector Amplifier 1132
16.5.4	A Supply-Independent MOS Reference Cell 1060	17.3.6	Estimate of ω_L for the Common-Drain Amplifier 1132
16.6	The Bandgap Reference 1062	17.4	Transistor Models at High Frequencies 1133
16.7	The Current Mirror as an Active Load 1066	17.4.1	Frequency-Dependent Hybrid-Pi Model for the Bipolar Transistor 1133
16.7.1	CMOS Differential Amplifier with Active Load 1066	17.4.2	Modeling C_π and C_μ in SPICE 1134
16.7.2	Bipolar Differential Amplifier with Active Load 1073	17.4.3	Unity-Gain Frequency f_T 1134
16.8	Active Loads in Operational Amplifiers 1077	17.4.4	High-Frequency Model for the FET 1137
16.8.1	CMOS Op Amp Voltage Gain 1077	17.4.5	Modeling C_{GS} and C_{GD} in SPICE 1138
16.8.2	dc Design Considerations 1078	17.4.6	Channel Length Dependence of f_T 1138
16.8.3	Bipolar Operational Amplifiers 1080	17.4.7	Limitations of the High-Frequency Models 1140
16.8.4	Input Stage Breakdown 1081	17.5	Base and Gate Resistances in the Small-Signal Models 1140
16.9	The μ A741 Operational Amplifier 1082	17.5.1	Effect of Base and Gate Resistances on Midband Amplifiers 1141
16.9.1	Overall Circuit Operation 1082	17.6	High-Frequency Common-Emitter and Common-Source Amplifier Analysis 1142
16.9.2	Bias Circuitry 1083	17.6.1	The Miller Effect 1144
16.9.3	dc Analysis of the 741 Input Stage 1084	17.6.2	Common-Emitter and Common-Source Amplifier High-Frequency Response 1146
16.9.4	ac Analysis of the 741 Input Stage 1087	17.6.3	Direct Analysis of the Common-Emitter Transfer Characteristic 1148
16.9.5	Voltage Gain of the Complete Amplifier 1088	17.6.4	Poles of the Common-Emitter Amplifier 1149
16.9.6	The 741 Output Stage 1092	17.6.5	Dominant Pole for the Common-Source Amplifier 1152
16.9.7	Output Resistance 1094	17.6.6	Estimation of ω_H Using the Open-Circuit Time-Constant Method 1154
16.9.8	Short-Circuit Protection 1094	17.6.7	Common-Source Amplifier with Source Degeneration Resistance 1155
16.9.9	Summary of the μ A741 Operational Amplifier Characteristics 1094		
16.10	The Gilbert Analog Multiplier 1095		
	<i>Summary 1097</i>		
	<i>Key Terms 1098</i>		
	<i>References 1099</i>		
	<i>Problems 1099</i>		

CHAPTER 17

AMPLIFIER FREQUENCY RESPONSE 1113

17.1	Amplifier Frequency Response 1114
17.1.1	Low-Frequency Response 1115
17.1.2	Estimating ω_L in the Absence of a Dominant Pole 1115
17.1.3	High-Frequency Response 1118
17.1.4	Estimating ω_H in the Absence of a Dominant Pole 1118

17.2	Direct Determination of the Low-Frequency Poles and Zeros—the Common-Source Amplifier 1119
17.3	Estimation of ω_L Using the Short-Circuit Time-Constant Method 1124
17.3.1	Estimate of ω_L for the Common-Emitter Amplifier 1125
17.3.2	Estimate of ω_L for the Common-Source Amplifier 1129
17.3.3	Estimate of ω_L for the Common-Base Amplifier 1130
17.3.4	Estimate of ω_L for the Common-Gate Amplifier 1131
17.3.5	Estimate of ω_L for the Common-Collector Amplifier 1132
17.3.6	Estimate of ω_L for the Common-Drain Amplifier 1132
17.4	Transistor Models at High Frequencies 1133
17.4.1	Frequency-Dependent Hybrid-Pi Model for the Bipolar Transistor 1133
17.4.2	Modeling C_π and C_μ in SPICE 1134
17.4.3	Unity-Gain Frequency f_T 1134
17.4.4	High-Frequency Model for the FET 1137
17.4.5	Modeling C_{GS} and C_{GD} in SPICE 1138
17.4.6	Channel Length Dependence of f_T 1138
17.4.7	Limitations of the High-Frequency Models 1140
17.5	Base and Gate Resistances in the Small-Signal Models 1140
17.5.1	Effect of Base and Gate Resistances on Midband Amplifiers 1141
17.6	High-Frequency Common-Emitter and Common-Source Amplifier Analysis 1142
17.6.1	The Miller Effect 1144
17.6.2	Common-Emitter and Common-Source Amplifier High-Frequency Response 1146
17.6.3	Direct Analysis of the Common-Emitter Transfer Characteristic 1148
17.6.4	Poles of the Common-Emitter Amplifier 1149
17.6.5	Dominant Pole for the Common-Source Amplifier 1152
17.6.6	Estimation of ω_H Using the Open-Circuit Time-Constant Method 1154
17.6.7	Common-Source Amplifier with Source Degeneration Resistance 1155

17.6.8	Poles of the Common-Emitter with Emitter Degeneration Resistance 1157	
17.7	Common-Base and Common-Gate Amplifier High-Frequency Response 1160	
17.8	Common-Collector and Common-Drain Amplifier High-Frequency Response 1162	
17.8.1	Frequency Response of the Complementary Emitter Follower 1165	
17.9	Single-Stage Amplifier High-Frequency Response Summary 1166	
17.9.1	Amplifier Gain-Bandwidth Limitations 1167	
17.10	Frequency Response of Multistage Amplifiers 1168	
17.10.1	Differential Amplifier 1168	
17.10.2	The Common-Collector/Common-Base Cascade 1170	
17.10.3	High-Frequency Response of the Cascode Amplifier 1171	
17.10.4	Cutoff Frequency for the Current Mirror 1172	
17.10.5	Three-Stage Amplifier Example 1173	
17.11	Introduction to Radio Frequency Circuits 1181	
17.11.1	Radio Frequency Amplifiers 1182	
17.11.2	The Shunt-Peaked Amplifier 1182	
17.11.3	Single-Tuned Amplifier 1184	
17.11.4	Use of a Tapped Inductor—the Auto Transformer 1186	
17.11.5	Multiple Tuned Circuits—Synchronous and Stagger Tuning 1188	
17.11.6	Common-Source Amplifier with Inductive Degeneration 1189	
17.12	Mixers and Balanced Modulators 1193	
17.12.1	Introduction to Mixer Operation 1193	
17.12.2	A Single-Balanced Mixer 1194	
17.12.3	The Differential Pair as a Single-Balanced Mixer 1195	
17.12.4	A Double-Balanced Mixer 1197	
17.12.5	The Jones Mixer—a Double-Balanced Mixer/Modulator 1199	
	<i>Summary</i> 1203	
	<i>Key Terms</i> 1204	
	<i>References</i> 1204	
	<i>Problems</i> 1205	
CHAPTER 18		
TRANSISTOR FEEDBACK AMPLIFIERS AND OSCILLATORS 1217		
18.1	Basic Feedback System Review 1218	
18.1.1	Closed-Loop Gain 1218	
18.1.2	Closed-Loop Impedances 1219	
18.1.3	Feedback Effects 1219	
18.2	Feedback Amplifier Analysis at Midband 1221	
18.2.1	Closed-Loop Gain 1221	
18.2.2	Input Resistance 1222	
18.2.3	Output Resistance 1222	
18.2.4	Offset Voltage Calculation 1223	
18.3	Feedback Amplifier Circuit Examples 1224	
18.3.1	Series-Shunt Feedback—Voltage Amplifiers 1224	
18.3.2	Differential Input Series-Shunt Voltage Amplifier 1229	
18.3.3	Shunt-Shunt Feedback—Transresistance Amplifiers 1232	
18.3.4	Series-Series Feedback—Transconductance Amplifiers 1238	
18.3.5	Shunt-Series Feedback—Current Amplifiers 1241	
18.4	Review of Feedback Amplifier Stability 1244	
18.4.1	Closed-Loop Response of the Uncompensated Amplifier 1245	
18.4.2	Phase Margin 1246	
18.4.3	Higher Order Effects 1250	
18.4.4	Response of the Compensated Amplifier 1251	
18.4.5	Small-Signal Limitations 1253	
18.5	Single-Pole Operational Amplifier Compensation 1253	
18.5.1	Three-Stage Op-Amp Analysis 1254	
18.5.2	Transmission Zeros in FET Op Amps 1256	
18.5.3	Bipolar Amplifier Compensation 1257	
18.5.4	Slew Rate of the Operational Amplifier 1258	
18.5.5	Relationships between Slew Rate and Gain-Bandwidth Product 1259	
18.6	High-Frequency Oscillators 1268	
18.6.1	The Colpitts Oscillator 1269	

- 18.6.2 The Hartley Oscillator 1270
 - 18.6.3 Amplitude Stabilization in *LC* Oscillators 1271
 - 18.6.4 Negative Resistance in Oscillators 1271
 - 18.6.5 Negative G_m Oscillator 1272
 - 18.6.6 Crystal Oscillators 1274
- Summary* 1278
Key Terms 1280
References 1280
Problems 1280

APPENDICES

- A Standard Discrete Component Values 1291
 - B Solid-State Device Models and SPICE Simulation Parameters 1294
 - C Two-Port Review 1299
- Index 1303