

Contents

Preface to First Edition	xiii
Preface	xv
About the Author	xvii
1 Introduction to Optical Communications	1
1.1 Brief History	1
1.2 Generic Optical System	2
1.3 Design Challenges	5
1.4 State of the Art	6
2 Basic Concepts	8
2.1 Properties of Random Binary Data	8
2.2 Generation of Random Data	12
2.3 Data Formats	14
2.3.1 NRZ and RZ Data	14
2.3.2 8B/10B Coding	14
2.4 Effect of Bandwidth Limitation on Random Data	16
2.4.1 Effect of Low-Pass Filtering	16
2.4.2 Eye Diagrams	16
2.4.3 Effect of High-Pass Filtering	18
2.5 Effect of Noise on Random Data	21
2.6 Phase Noise and Jitter	24
2.6.1 Phase Noise	24
2.6.2 Jitter	27
2.6.3 Relationship Between Phase Noise and Jitter	28
2.6.4 Jitter Due to Additive Noise	28
2.7 Transmission Lines	30
2.7.1 Ideal Transmission Lines	30
2.7.2 Lossy Transmission Lines	33
3 Optical Devices	36
3.1 Laser Diodes	36
3.1.1 Operation of Lasers	38

3.1.2	Types of Lasers	40
3.1.3	Properties of Lasers	42
3.1.4	External Modulation	45
3.2	Optical Fibers	46
3.2.1	Fiber Loss	47
3.2.2	Fiber Dispersion	48
3.3	Photodiodes	55
3.3.1	Responsivity and Efficiency	55
3.3.2	PIN Diodes	56
3.3.3	Avalanche Photodiodes	57
3.4	Optical Systems	58
4	Transimpedance Amplifiers	62
4.1	General Considerations	62
4.1.1	TIA Performance Parameters	64
4.1.2	SNR Calculations	69
4.1.3	Noise Bandwidth	72
4.2	Open-Loop TIAs	73
4.2.1	Low-Frequency Behavior	73
4.2.2	High-Frequency Behavior	81
4.3	Feedback TIAs	87
4.3.1	First-Order TIA	87
4.3.2	Second-Order TIA	89
4.4	Supply Rejection	97
4.5	Differential TIAs	100
4.6	High-Performance Techniques	103
4.6.1	Gain Boosting	103
4.6.2	Capacitive Coupling	105
4.6.3	Feedback TIAs	106
4.6.4	Inductive Peaking	110
4.7	Automatic Gain Control	114
4.8	Case Studies	118
4.9	New Developments in TIA Design	122
5	Limiting Amplifiers and Output Buffers	130
5.1	General Considerations	130
5.1.1	Performance Parameters	130
5.1.2	Cascaded Gain Stages	132
5.1.3	AM/PM Conversion	136
5.2	Broadband Techniques	138
5.2.1	Inductive Peaking	138
5.2.2	Capacitive Degeneration	140
5.2.3	Cherry-Hooper Amplifier	143
5.2.4	f_T Doublers	147

5.3	Output Buffers	149
5.3.1	Differential Signaling	149
5.3.2	Double Termination	153
5.3.3	Predriver Design	156
5.4	Distributed Amplification	159
5.4.1	Monolithic Transmission Lines	159
5.4.2	Distributed Amplifiers	163
5.4.3	Distributed Amplifiers with Lumped Devices	170
5.5	Other Broadband Techniques	171
5.5.1	T-Coil Peaking	171
5.5.2	Negative Capacitance	174
5.5.3	Active Feedback	178
5.5.4	Triple-Resonance Peaking	180
6	Oscillator Fundamentals	185
6.1	General Considerations	185
6.2	Ring Oscillators	187
6.3	LC Oscillators	198
6.3.1	Crossed-Coupled Oscillator	201
6.3.2	Colpitts Oscillator	204
6.3.3	One-Port Oscillators	207
6.4	Voltage-Controlled Oscillators	211
6.4.1	Tuning in Ring Oscillators	214
6.4.2	Tuning in LC Oscillators	222
6.5	Mathematical Model of VCOs	227
7	LC Oscillators	233
7.1	Monolithic Inductors	233
7.1.1	Loss Mechanisms	235
7.1.2	Inductor Modeling	239
7.1.3	Inductor Design Guidelines	242
7.2	Monolithic Varactors	246
7.3	Basic LC Oscillators	248
7.3.1	Differential Control	251
7.3.2	Design Procedure	253
7.4	Quadrature Oscillators	255
7.4.1	In-Phase Coupling	257
7.4.2	Antiphase Coupling	259
7.5	Distributed Oscillators	261
8	Phase-Locked Loops	264
8.1	Simple PLL	264
8.1.1	Phase Detector	264
8.1.2	Basic PLL Topology	265
8.1.3	Dynamics of Simple PLL	274

8.2	Charge-Pump PLLs	280
8.2.1	Problem of Lock Acquisition	281
8.2.2	Phase/Frequency Detector and Charge Pump	282
8.2.3	Basic Charge-Pump PLL	286
8.3	Nonideal Effects in PLLs	293
8.3.1	PFD/CP Nonidealities	293
8.3.2	Jitter in PLLs	297
8.4	Delay-Locked Loops	300
8.5	Applications	302
8.5.1	Frequency Multiplication and Synthesis	303
8.5.2	Skew Reduction	305
8.5.3	Jitter Reduction	306
9	Clock and Data Recovery	308
9.1	General Considerations	308
9.2	Phase Detectors for Random Data	320
9.2.1	Hogge Phase Detector	320
9.2.2	Alexander Phase Detector	324
9.2.3	Half-Rate Phase Detectors	329
9.3	Frequency Detectors for Random Data	333
9.4	CDR Architectures	338
9.4.1	Full-Rate Referenceless Architecture	338
9.4.2	Dual-VCO Architecture	339
9.4.3	Dual-Loop Architecture with External Reference	341
9.4.4	Quarter-Rate Phase Detectors	342
9.5	Jitter in CDR Circuits	344
9.5.1	Jitter Transfer	345
9.5.2	Jitter Generation	349
9.5.3	Jitter Tolerance	351
10	Multiplexers and Laser Drivers	356
10.1	Multiplexers	356
10.1.1	2-to-1 MUX	356
10.1.2	MUX Architectures	361
10.2	Frequency Dividers	364
10.2.1	Flipflop Dividers	364
10.2.2	Miller Divider	372
10.3	Laser and Modulator Drivers	374
10.3.1	Performance Parameters	374
10.4	Design Principles	378
10.4.1	Power Control	384
10.5	New Developments in Laser Driver Design	385
11	Burst-Mode Circuits	393
11.1	Passive Optical Networks	393

11.2	Burst-Mode TIAs	395
11.2.1	TIA with Top and Bottom Hold	396
11.2.2	Burst-Mode TIA Variants	400
11.2.3	Offset Correction in Limiting Amplifiers	402
11.3	Burst-Mode CDR Circuits	404
11.3.1	Effect of Finite Delays	405
11.3.2	Effect of Frequency Mismatch and Offset	406
11.3.3	Jitter Characteristics	410
11.4	Alternative BM CDR Architectures	413

Index**417**