

Contents

Foreword	v
Preface	vii
1 Introduction	1
1.1 How PI Lays Out a Chip: An Example	3
2 Preliminaries	27
2.1 Specifications for the PI System	27
2.2 Terminology	31
3 The Placement Framework	37
3.1 Overview of PI's Placement Heuristics	37
3.2 PI's Placement Problem	39
3.3 The Placement Tree	40
3.4 How PI Refines the Placement Tree	45
4 Chip Estimation and Pad Placement	53
4.1 Estimating Chip Size and Shape	53
4.2 Pad Placement	55
5 Logic Placement	59
5.1 Top-Down Mincut Partitioning	59
5.2 Module Orientation	68
5.3 Bottom-Up Hardening	70
5.4 Additional Placement Heuristics	78
5.5 Open Placement Problems	84
6 Power-Ground Routing	93
6.1 Overview of Power-Ground Routing	93
6.2 The Hamiltonian Circuit Heuristic	95

6.3	Calculating Current Requirements	98
7	Signal Routing	99
7.1	Overview of Signal Routing	99
7.2	Channel Definition	100
7.3	Global Routing	102
7.4	Crossing Placement	103
7.5	Channel Routing	108
8	Resizing	114
8.1	Overview of Resizing	114
8.2	Gathering the Constraints	117
8.3	Solving the Constraint Graphs	118
8.4	How PI Converges on a Solution	120
9	The MIT Implementation of PI	121
9.1	Objectives	121
9.2	Major Design Decisions	122
9.3	Critique	123
9.4	Source Code, Contributors, and Documentation	127
10	Related Layout Systems	133
10.1	2PI at General Electric	133
10.2	EC-PI at the Technion	140
10.3	Selected Other Layout Systems	146
11	Conclusion	151
	Bibliography	155
	Basic Sources	156
	Mathematics and Computer Science	159
	VLSI Theory	163
	Placement	165
	Routing	169
	Compaction	172
	The PI System	173
	Other Placement and Routing Systems	175
	Layouts of Specific Circuits	177
	Other Works	178
	Index	181