# PHASE-LOCKED LOOP CIRCUIT DESIGN

Dan H. Wolaver Worcester Polytechnic Institute



P T R Prentice Hall, Englewood Cliffs, New Jersey 07632

## CONTENTS

#### PREFACE

#### 1. INTRODUCTION

- 1-1 Carrier Recovery 2
- 1-2 Clock Recovery 3
- 1-3 Tracking Filter 3
- 1-4 Frequency Demodulation 4
- 1-5 Phase Demodulation 5
- 1-6 Phase Modulation 5
- 1-7 Frequency Synthesis 6
- 1-8 Organization of Text 7
- 1-9 Other Information on Phase-Locked Loops 7

### 2. PHASE-LOCKED LOOP BASICS

- 2-1 Phase-Locked Loop Characteristics 9
- 2-2 Phase Detector Characteristics 11

9

ix

vi

- 2-3 VCO Characteristics 11
- 2-4 Linear Model of PLL 13
- 2-5 Static Phase Error 14
- 2-6 PLL Bandwidth 15
- 2-7 Loop Filter 20
- 2-8 Static Phase Error with Loop Filter 22

#### 3. LOOP FILTERS

- 3-1 Active Loop Filter 26
- 3-2 Static Phase Error with Active Loop Filter 28
- 3-3 Alternative Active Loop Filter Designs 29
- 3-4 Active Loop Filter Offsets 31
- 3-5 PLL Frequency Response 32
- 3-6 PLL Step Response 36
- 3-7 Limited Loop Filter Bandwidth 38
- 3-8 Phase Error Response 43

#### 4. PHASE DETECTORS

- 4-1 Four-Quadrant Multipliers 47
- 4-2 Gilbert Multiplier 50
- 4-3 Phase Detector Figure of Merit 52
- 4-4 Double Balanced Multiplier 52
- 4-5 Triangular Phase Detector Characteristic 54
- 4-6 Exclusive-OR Phase Detector 55
- 4-7 Two-State Phase Detector 59
- 4-8 Three-State Phase Detector 61
- 4-9 Z-State Phase Detector 65
- 4-10 Sample-and-Hold Phase Detector 67
- 4-11 Extended Range: Frequency Division 68
- 4-12 Extended Range: n-State Phase Detector 68
- 4-13 Modified Phase Detector Characteristic 75

#### 5. VOLTAGE-CONTROLLED OSCILLATOR

- 5-1 Properties of VCOs 81
- 5-2 Voltage-Controlled Multivibrators 83
- 5-3 Resonant VCOs 86
- 5-4 Modulation Bandwidth 91
- 5-5 Q of the Resonant Circuit 92
- 5-6 Crystal VCOs 94
- 5-7 Injection in Multivibrator VCOs 97

25

47

5-8	Injection in Resonant VCOs	100
5-9	PLL Behavior with Injection	102
5-10	Spectral Purity 105	

#### 6. NOISE

6-1	Power Spectral Density 107	
6-2	Noise Bandwidth 109	
6-3	Noise-Induced Phase 111	
6-4	Output Phase Noise Due to Input Noise	116
6-5	VCO Phase Noise 120	
6-6	Output Phase Noise Due to VCO Noise	126
6-7	Output Phase Noise Due to Both Nosie	
	Sources 128	
6-8	Cycle Slips 131	

#### 7. MAINTAINING LOCK

7-	1 ]	Hol	d-I	n F	Rang	ge	13:	5
					2			

- 7-2 Input Frequency Deviation  $\Delta \omega_i$  136
- 7-3 Lock-In Frequency  $\omega_L$  138
- 7-4 Transfer Function from  $\Delta \omega_i$  to  $\theta_e$  142
- 7-5 Handling a Frequency Step 143
- 7-6 Handling a Frequency Ramp 145
- 7-7 Handling Sinusoidal FM 148
- 7-8 Handling Random FM 151

#### 8. LOCK ACQUISITION

8-1	Self Acquisition: Active Loop Filter 157
	8-1-1 Pull-In Voltage v <sub>p</sub> 157
	8-1-2 Pull-In Time $T_p$ 160
	8-1-3 Pull-In Range $\omega_{\rm p}$ 163
8-2	Self Acquisition: Passive Loop Filter 164
8-3	Acquisition with a Pole at $\omega_3$ 168
8-4	Acquisition with a Three-State PD 171
8-5	Aided Acquisition with a Three-State PD 174
8-6	Rotational Frequency Detector 177

#### 9. MODULATION AND DEMODULATION

9-1	Phase N	Iodulation	185		
	9-1-1	Bandwid	th, Phase	and	Frequency
		Ranges	186		

107

9-1-3	Spur	ious	Modulation	with	a	Pole	at
	ω	189					

- 9-2 Phase Demodulation 192
- 9-3 Phase Demodulation with No Carrier 195
  - 9-3-1 Squaring Loop 196
  - 9-3-2 Remodulator and Costas Loop 200
- 9-4 Frequency Modulation 202
- 9-5 Frequency Demodulation 205
- 10. CLOCK RECOVERY
  - 10-1 Data Formats and Spectra 212
  - 10-2 Conversion from NRZ and RZ Data 213
  - 10-3 Phase Detectors for RZ Data 216
  - 10-4 Pattern-Dependent Jitter 218
  - 10-5Phase Detectors for NRZ Data 220
  - 10-6 Offset Jitter 220
  - 10-7 Jitter Accumulation 230

#### 11. FREQUENCY SYNTHESIZERS

- 11-1 Single-Loop Synthesizer 239
- 11-2 Choosing the Bandwidth K 240
- 11-3 Synthesizer with Mixer 241
- 11-4 Spurious Modulation 242
- 11-5 Divided Output 248
- 11-6 Pull-In Time 248
- 11-7 Multiplexed Output 250
- 11-8 Multiple-Loop Synthesizer 250
- 11-9 Phase Noise 252
- 11-10 Prescaling 257

LIST OF SYMBOLS

INDEX

261

239

211