

# THE x86 PC

## Assembly Language, Design, and Interfacing

Fifth Edition

Muhammad Ali Mazidi

Janice Gillispie Mazidi

Danny Causey

**PEARSON**

Boston Columbus Indianapolis New York San Francisco Upper Saddle River

Amsterdam Cape Town Dubai London Madrid Milan Munich Paris Montreal Toronto

Delhi Mexico City Sao Paulo Sydney Hong Kong Seoul Singapore Taipei Tokyo

# CONTENTS

<b>CHAPTER 0: INTRODUCTION TO COMPUTING</b>	<b>1</b>
SECTION 0.1: NUMBERING AND CODING SYSTEMS	2
SECTION 0.2: DIGITAL PRIMER	9
SECTION 0.3: INSIDE THE COMPUTER	13
<b>CHAPTER 1: THE x86 MICROPROCESSOR</b>	<b>23</b>
SECTION 1.1: BRIEF HISTORY OF THE x86 FAMILY	24
SECTION 1.2: INSIDE THE 8088/86	27
SECTION 1.3: INTRODUCTION TO ASSEMBLY PROGRAMMING	30
SECTION 1.4: INTRODUCTION TO PROGRAM SEGMENTS	33
SECTION 1.5: THE STACK	39
SECTION 1.6: FLAG REGISTER	43
SECTION 1.7: x86 ADDRESSING MODES	46
<b>CHAPTER 2: ASSEMBLY LANGUAGE PROGRAMMING</b>	<b>55</b>
SECTION 2.1: DIRECTIVES AND A SAMPLE PROGRAM	56
SECTION 2.2: ASSEMBLE, LINK, AND RUN A PROGRAM	60
SECTION 2.3: MORE SAMPLE PROGRAMS	63
SECTION 2.4: CONTROL TRANSFER INSTRUCTIONS	68
SECTION 2.5: DATA TYPES AND DATA DEFINITION	72
SECTION 2.6: FULL SEGMENT DEFINITION	77
SECTION 2.7: FLOWCHARTS AND PSEUDOCODE	83
<b>CHAPTER 3: ARITHMETIC AND LOGIC INSTRUCTIONS AND PROGRAMS</b>	<b>91</b>
SECTION 3.1: UNSIGNED ADDITION AND SUBTRACTION	92
SECTION 3.2: UNSIGNED MULTIPLICATION AND DIVISION	98
SECTION 3.3: LOGIC INSTRUCTIONS	102
SECTION 3.4: BCD AND ASCII CONVERSION	111
SECTION 3.5: ROTATE INSTRUCTIONS	118
SECTION 3.6: BITWISE OPERATORS IN THE C LANGUAGE	121
<b>CHAPTER 4: INT 21H AND INT 10H PROGRAMMING AND MACROS</b>	<b>129</b>
SECTION 4.1: BIOS INT 10H PROGRAMMING	130
SECTION 4.2: DOS INTERRUPT 21H	137
SECTION 4.3: WHAT IS A MACRO AND HOW IS IT USED?	147
<b>CHAPTER 5: KEYBOARD AND MOUSE PROGRAMMING</b>	<b>161</b>
SECTION 5.1: INT 16H KEYBOARD PROGRAMMING	162
SECTION 5.2: MOUSE PROGRAMMING WITH INT 33H	166
<b>CHAPTER 6: SIGNED NUMBERS, STRINGS, AND TABLES</b>	<b>175</b>
SECTION 6.1: SIGNED NUMBER ARITHMETIC OPERATIONS	176
SECTION 6.2: STRING AND TABLE OPERATIONS	186
<b>CHAPTER 7: MODULES AND MODULAR PROGRAMMING</b>	<b>195</b>
SECTION 7.1: WRITING AND LINKING MODULES	196
SECTION 7.2: SOME VERY USEFUL MODULES	205
SECTION 7.3: PASSING PARAMETERS AMONG MODULES	211

<b>CHAPTER 8: 32-BIT PROGRAMMING FOR x86</b>	<b>217</b>
SECTION 8.1: 32-BIT PROGRAMMING IN x86	218
<b>CHAPTER 9: 8088, 80286 MICROPROCESSORS AND ISA BUS</b>	<b>227</b>
SECTION 9.1: 8088 MICROPROCESSOR	228
SECTION 9.2: 8284 AND 8288 SUPPORTING CHIPS	233
SECTION 9.3: 8-BIT SECTION OF ISA BUS	238
SECTION 9.4: 80286 MICROPROCESSOR	242
SECTION 9.5: 16-BIT ISA BUS	246
<b>CHAPTER 10: MEMORY AND MEMORY INTERFACING</b>	<b>255</b>
SECTION 10.1: SEMICONDUCTOR MEMORIES	256
SECTION 10.2: MEMORY ADDRESS DECODING	265
SECTION 10.3: IBM PC MEMORY MAP	269
SECTION 10.4: DATA INTEGRITY IN RAM AND ROM	273
SECTION 10.5: 16-BIT MEMORY INTERFACING	278
<b>CHAPTER 11: 8255 I/O PROGRAMMING</b>	<b>289</b>
SECTION 11.1: 8088 INPUT/OUTPUT INSTRUCTIONS	290
SECTION 11.2: I/O ADDRESS DECODING AND DESIGN	292
SECTION 11.3: I/O ADDRESS MAP OF x86 PCs	294
SECTION 11.4: PROGRAMMING AND INTERFACING THE 8255	299
<b>CHAPTER 12: INTERFACING TO LCD, MOTOR, ADC, AND SENSOR</b>	<b>315</b>
SECTION 12.1: INTERFACING TO AN LCD	316
SECTION 12.2: INTERFACING TO A STEPPER MOTOR	326
SECTION 12.3: INTERFACING TO A DAC	332
SECTION 12.4: INTERFACING TO ADC CHIPS AND SENSORS	336
<b>CHAPTER 13: 8253/54 TIMER</b>	<b>349</b>
SECTION 13.1: 8253/54 TIMER	350
SECTION 13.2: x86 PC 8253/54 TIMER CONNECTION AND PROGRAMMING	354
SECTION 13.3: GENERATING MUSIC ON THE x86 PC	359
<b>CHAPTER 14: INTERRUPTS IN x86 PC</b>	<b>367</b>
SECTION 14.1: 8088/86 INTERRUPTS	368
SECTION 14.2: x86 PC AND INTERRUPT ASSIGNMENT	374
SECTION 14.3: 8259 PROGRAMMABLE INTERRUPT CONTROLLER	377
SECTION 14.4: USE OF THE 8259 CHIP IN x86 PCs	387
SECTION 14.5: MORE ON INTERRUPTS IN x86 PCs	393
<b>CHAPTER 15: DIRECT MEMORY ACCESS AND DMA CHANNELS IN x86 PC</b>	<b>401</b>
SECTION 15.1: CONCEPT OF DMA	402
SECTION 15.2: 8237 DMA CHIP PROGRAMMING	404
SECTION 15.3: 8237 DMA INTERFACING IN THE IBM PC	413
SECTION 15.4: DMA IN x86 PCs	417

<b>CHAPTER 16: VIDEO AND VIDEO ADAPTERS</b>	<b>423</b>
SECTION 16.1: PRINCIPLES OF MONITORS AND VIDEO MODES	424
SECTION 16.2: TEXT MODE PROGRAMMING AND VIDEO RAM	433
SECTION 16.3: GRAPHICS AND GRAPHICS PROGRAMMING	440
<b>CHAPTER 17: SERIAL PORT PROGRAMMING WITH ASSEMBLY AND C#</b>	<b>447</b>
SECTION 17.1: BASICS OF SERIAL COMMUNICATION	448
SECTION 17.2: PROGRAMMING x86 PC COM PORTS USING ASSEMBLY AND C#	455
<b>CHAPTER 18: KEYBOARD AND PRINTER INTERFACING</b>	<b>463</b>
SECTION 18.1: INTERFACING THE KEYBOARD TO THE CPU	464
SECTION 18.2: PC KEYBOARD INTERFACING AND PROGRAMMING	468
SECTION 18.3: PRINTER AND PRINTER INTERFACING IN THE IBM PC	478
<b>CHAPTER 19: HARD DISKS</b>	<b>491</b>
SECTION 19.1: HARD DISK ORGANIZATION AND PERFORMANCE	492
<b>CHAPTER 20: THE IEEE FLOATING POINT AND x87 MATH PROCESSORS</b>	<b>503</b>
SECTION 20.1: MATH COPROCESSOR AND IEEE FLOATING-POINT STANDARDS	504
SECTION 20.2: x87 INSTRUCTIONS AND PROGRAMMING	508
SECTION 20.3: x87 INSTRUCTIONS	519
<b>CHAPTER 21: 386 MICROPROCESSOR: REAL vs. PROTECTED MODE</b>	<b>529</b>
SECTION 21.1: 80386 IN REAL MODE	530
SECTION 21.2: 80386: A HARDWARE VIEW	539
SECTION 21.3: 80386 PROTECTED MODE	545
<b>CHAPTER 22: HIGH-SPEED MEMORY DESIGN AND CACHE</b>	<b>559</b>
SECTION 22.1: MEMORY CYCLE TIME OF THE x86	560
SECTION 22.2: PAGE AND STATIC COLUMN DRAMS	562
SECTION 22.3: CACHE MEMORY	570
SECTION 22.4: SDRAM, DDR RAM, AND RAMBUS MEMORIES	578
<b>CHAPTER 23: PENTIUM AND RISC PROCESSORS</b>	<b>589</b>
SECTION 23.1: THE 80486 MICROPROCESSOR	590
SECTION 23.2: INTEL'S PENTIUM	596
SECTION 23.3: RISC ARCHITECTURE	602
SECTION 23.4: PENTIUM PRO PROCESSOR	609
SECTION 23.5: MMX TECHNOLOGY	613
<b>CHAPTER 24: THE EVOLUTION OF x86: FROM 32-BIT TO 64-BIT</b>	<b>625</b>
SECTION 24.1: x86 PENTIUM EVOLUTION	626
SECTION 24.2: 64-BIT PROCESSORS AND VISTA FOR x86	632

<b>CHAPTER 25: SYSTEM DESIGN ISSUES AND FAILURE ANALYSIS</b>	<b>637</b>
SECTION 25.1: OVERVIEW OF IC TECHNOLOGY	638
SECTION 25.2: IC INTERFACING AND SYSTEM DESIGN ISSUES	644
<b>CHAPTER 26: ISA, PC104, AND PCI BUSES</b>	<b>659</b>
SECTION 26.1: ISA BUS MEMORY SIGNALS	660
SECTION 26.2: I/O BUS TIMING IN ISA BUS	668
SECTION 26.3: PCI BUS	676
<b>CHAPTER 27: USB PORT PROGRAMMING</b>	<b>687</b>
SECTION 27.1: USB PORTS: AN OVERVIEW	688
SECTION 27.2: USB PORT EXPANSION AND POWER MANAGEMENT	689
SECTION 27.3: USB PORT PROGRAMMING	694
<b>APPENDIX A: DEBUG PROGRAMMING</b>	<b>699</b>
SECTION A.1: ENTERING AND EXITING DEBUG	700
SECTION A.2: EXAMINING AND ALTERING REGISTERS	700
SECTION A.3: CODING AND RUNNING PROGRAMS IN DEBUG	702
SECTION A.4: DATA MANIPULATION IN DEBUG	706
SECTION A.5: EXAMINING/ALTERING THE FLAG REGISTER IN DEBUG	710
<b>APPENDIX B: x86 INSTRUCTIONS DESCRIPTION</b>	<b>715</b>
SECTION B.1: THE 8086 INSTRUCTION SET	716
<b>APPENDIX C: ASSEMBLER DIRECTIVES AND NAMING RULES</b>	<b>739</b>
SECTION C.1: x86 ASSEMBLER DIRECTIVES	740
SECTION C.2: RULES FOR LABELS AND RESERVED NAMES	750
<b>APPENDIX D: INTERRUPT CALLS AND LEGACY SOFTWARE</b>	<b>753</b>
SECTION D.1: 21H INTERRUPTS	754
SECTION D.2: MOUSE INTERRUPTS 33H	755
SECTION D.3: INT 10H	759
SECTION D.4: INT 12H	765
SECTION D.5: INT 14H	765
SECTION D.6: INT 16H -- KEYBOARD	767
SECTION D.7: INT 1AH	770
<b>APPENDIX E: I/O ADDRESS MAP</b>	<b>773</b>
SECTION E.1: ORIGINAL 80286 IBM PC I/O ADDRESS MAP	773
SECTION E.2: Dell x86 PC I/O ADDRESS MAP	774
<b>APPENDIX F: ASCII CODES</b>	<b>777</b>
<b>INDEX</b>	<b>779</b>