

*MOSFET Models  
for VLSI Circuit  
Simulation*

*Theory and Practice*

*N. Arora*

*Springer-Verlag Wien New York*

# Contents

List of Symbols XVII

Acronyms XXII

- 1 Overview 1
  - 1.1 Circuit Design with MOSFETs 3
  - 1.2 MOSFET Modeling 5
  - 1.3 Model Parameter Determination 9
  - 1.4 Interconnect Modeling 10
  - 1.5 Subjects Covered 11
- References 11
  
- 2 Review of Basic Semiconductor and *pn* Junction Theory 15
  - 2.1 Energy Band Model 15
  - 2.2 Intrinsic Semiconductor 17
    - 2.2.1 Fermi level 19
  - 2.3 Extrinsic or Doped Semiconductor 21
    - 2.3.1 Generation-Recombination 25
    - 2.3.2 Quasi-Fermi Level 27
  - 2.4 Electrical Conduction 28
    - 2.4.1 Carrier Mobility 28
    - 2.4.2 Resistivity and Sheet Resistance 33
    - 2.4.3 Transport Equations 36
    - 2.4.4 Continuity Equation 37
    - 2.4.5 Poisson's Equation 38
  - 2.5 *pn* Junction at Equilibrium 39
    - 2.5.1 Built-in Potential 42
    - 2.5.2 Depletion Width 43
  - 2.6 Diode Current-Voltage Characteristics 46
    - 2.6.1 Limitation of the Diode Current Model 48
    - 2.6.2 Bulk Resistance 51
    - 2.6.3 Junction Breakdown Voltage 52

- 2.7 Diode Dynamic Behavior 53
  - 2.7.1 Junction Capacitance 53
  - 2.7.2 Diffusion Capacitance 56
  - 2.7.3 Small Signal Conductance 57
- 2.8 Real *pn* Junction 58
- 2.9 Diode Circuit Model 61
- 2.10 Temperature Dependent Diode Model Parameters 64
  - 2.10.1 Temperature Dependence of  $I_s$  64
  - 2.10.2 Temperature Dependence of  $\phi_{bi}$  66
  - 2.10.3 Temperature Dependence of  $C_{j0}$  66
- References 67
  
- 3 MOS Transistor Structure and Operation 69
  - 3.1 MOSFET Structure 69
  - 3.2 MOSFET Characteristics 73
    - 3.2.1 Punchthrough 81
    - 3.2.2 MOSFET Capacitances 82
    - 3.2.3 Small-Signal Behavior 84
    - 3.2.4 Device Speed 86
  - 3.3 MOSFET Scaling 87
  - 3.4 Hot-Carrier Effects 90
  - 3.5 VLSI Device Structures 93
    - 3.5.1 Gate Material 93
    - 3.5.2 Nonuniform Channel Doping 94
    - 3.5.3 Source-Drain Structures 95
    - 3.5.4 Device Isolation 98
    - 3.5.5 CMOS Process 99
  - 3.6 MOSFET Parasitic Elements 102
    - 3.6.1 Source-Drain Resistance 102
    - 3.6.2 Source/Drain Junction Capacitance 108
    - 3.6.3 Gate Overlap Capacitances 109
  - 3.7 MOSFET Length and Width Definitions 113
    - 3.7.1 Effective or Electrical Channel Length 113
    - 3.7.2 Effective or Electrical Channel Width 114
  - 3.8 MOSFET Circuit Models 115
- References 118
  
- 4 MOS Capacitor 121
  - 4.1 MOS Capacitor with No Applied Voltage 121
    - 4.1.1 Work Function 123
    - 4.1.2 Oxide Charges 127
    - 4.1.3 Flat Band Voltage 131
  - 4.2 MOS Capacitor at Non-Zero Bias 133
    - 4.2.1 Accumulation 135

- 4.2.2 Depletion 135
- 4.2.3 Inversion 138
- 4.3 Capacitance of MOS Structures 147
  - 4.3.1 Low Frequency C–V Plot 153
  - 4.3.2 High Frequency C–V Plot 154
  - 4.3.3 Deep Depletion C–V Plot 155
- 4.4 Deviation from Ideal C–V Curves 156
- 4.5 Anomalous C–V Curve (Polysilicon Depletion Effect) 159
- 4.6 MOS Capacitor Applications 161
- 4.7 Nonuniformly Doped Substrate and Flat Band Voltage 162
  - 4.7.1 Temperature Dependence of  $V_{fb}$  163
- References 165
  
- 5 Threshold Voltage 167
  - 5.1 MOSFET with Uniformly Doped Substrate 167
  - 5.2 Nonuniformly Doped MOSFET 177
    - 5.2.1 Enhancement Type Device 179
    - 5.2.2 Depletion Type Device 190
  - 5.3 Threshold Voltage Variations with Device Length and Width 194
    - 5.3.1 Short-Channel Effect 195
    - 5.3.2 Narrow-Width Effect 205
    - 5.3.3 Drain Induced Barrier Lowering (DIBL) Effect 210
    - 5.3.4 Small-Geometry Effect 219
  - 5.4 Temperature Dependence of the Threshold voltage 221
  - References 225
  
- 6 MOSFET DC Model 230
  - 6.1 Drain Current Calculations 230
  - 6.2 Pao-Sah Model 235
  - 6.3 Charge-Sheet Model 238
  - 6.4 Piece-Wise Drain Current Model for Enhancement Devices 243
    - 6.4.1 First Order Model 244
    - 6.4.2 Bulk-Charge Model 251
    - 6.4.3 Square-Root Approximation 253
    - 6.4.4 Drain Current Equation with Square-Root Approximation 257
    - 6.4.5 Subthreshold Region Model 259
    - 6.4.6 Limitations of the Model 267
  - 6.5 Drain Current Model for Depletion Devices 270
  - 6.6 Effective Mobility 276
    - 6.6.1 Mobility Degradation Due to the Gate Voltage 277
    - 6.6.2 Mobility Degradation Due to the Drain Voltage 284

- 6.7 Short-Geometry Models 287
  - 6.7.1 Linear Region Model 289
  - 6.7.2 Saturation Voltage 291
  - 6.7.3 Saturation Region—Channel Length Modulation 295
  - 6.7.4 Subthreshold Model 305
  - 6.7.5 Continuous Model 307
- 6.8 Impact of Source-Drain Resistance on Drain Current 310
- 6.9 Temperature Dependence of the Drain Current 313
  - 6.9.1 Temperature Dependence of Mobility 314
- References 318
  
- 7 Dynamic Model 325
  - 7.1 Intrinsic Charges and Capacitances 325
    - 7.1.1 Meyer Model 328
    - 7.1.2 Drawbacks of the Meyer Model 334
  - 7.2 Charge-Based Capacitance Model 337
  - 7.3 Long-Channel Charge Model 340
    - 7.3.1 Capacitances 347
  - 7.4 Short-Channel Charge Model 352
    - 7.4.1 Capacitances 356
  - 7.5 Limitations of the Quasi-Static Model 359
  - 7.6 Small-Signal Model Parameters 360
- References 364
  
- 8 Modeling Hot-Carrier Effects 366
  - 8.1 Substrate Current Model 367
  - 8.2 Gate Current Model 374
  - 8.3 Correlation of Gate and Substrate Current 382
  - 8.4 Mechanism of MOSFET Degradation 383
  - 8.5 Measure of Degradation—Device Lifetime 388
  - 8.6 Impact of Degradation on Circuit Performance 394
  - 8.7 Temperature Dependence of Device Degradation 396
- References 398
  
- 9 Data Acquisition and Model Parameter Measurements 402
  - 9.1 Data Acquisition 403
    - 9.1.1 Data for DC Models 410
    - 9.1.2 Data for AC Models 414
    - 9.1.3 MOS Capacitor C–V Measurement 418
  - 9.2 Gate-Oxide Capacitance Measurement 421
    - 9.2.1 Optical Method—Ellipsometry 421
    - 9.2.2 Electrical Method 422
  - 9.3 Measurement of Doping Profile in Silicon 427
    - 9.3.1 Capacitance–Voltage Method 428
    - 9.3.2 DC Method 436

9.4	Measurement of Threshold Voltage	438
9.5	Determination of Body Factor $\gamma$	443
9.6	Flat Band Voltage	445
9.7	Drain Induced Barrier Lowering (DIBL) Parameter	445
9.8	Determination of Subthreshold Slope	447
9.9	Carrier Inversion Layer Mobility Measurement	448
9.9.1	Split-CV Method	452
9.10	Determination of Effective Channel Length and Width	457
9.10.1	Drain Current Methods of Determination $\Delta L$	458
9.10.2	Capacitance Method of Determining $\Delta L$	468
9.10.3	Methods of Determining $\Delta W$	470
9.11	Determination of Drain Saturation Voltage	472
9.12	Measurement of MOSFET Intrinsic Capacitances	477
9.12.1	On-Chip Methods	477
9.12.2	Off-Chip Methods	481
9.13	Measurement of Gate Overlap Capacitance	484
9.14	Measurement of MOSFET Source/Drain Diode Junction Parameters	489
9.14.1	Diode Saturation or Reverse Current $I_s$	489
9.14.2	Junction Capacitance	493
	References	494
10	Model Parameter Extraction Using Optimization Method	501
10.1	Model Parameter Extraction	501
10.2	Basics Definitions in Optimization	504
10.3	Optimization Methods	510
10.3.1	Constrained Optimization	515
10.3.2	Multiple Response Optimization	518
10.4	Some Remarks on Parameter Extraction Using Optimization Technique	521
10.5	Confidence Limits on Estimated Model Parameter	522
10.5.1	Examples of Redundant Parameters	527
10.6	Parameter Extraction Using Optimizer	531
10.6.1	Drain Current Model Parameter Extraction	532
10.6.2	MOSFET AC Model Parameter Extraction	533
	References	534
11	SPICE Diode and MOSFET Models and Their Parameters	536
11.1	Diode Model	536
11.2	MOSFET Level 1 Model	542
11.2.1	DC Model	542
11.2.2	Capacitance Model	543
11.3	MOSFET Level 2 Model	548
11.3.1	DC Model	548
11.3.2	Capacitance Model	552

11.4	MOSFET Level 3 Model	554
11.4.1	DC Model	554
11.5	MOSFET Level 4 Model	556
11.5.1	DC Model	556
11.5.2	Capacitance Model	559
11.6	Comparison of the Four MOSFET Models	559
	References	561
12	Statistical Modeling and Worst-Case Design Parameters	563
12.1	Methods of Generating Worst Case Parameters	564
12.2	Model Parameter Sensitivity	566
12.2.1	Principal Factor Method	567
12.3	Statistical Analysis with Parameter Correlation	569
12.3.1	Principal Component Analysis	571
12.4	Factor Analysis	572
12.4.1	Factor Rotation	574
12.4.2	Regression Models	574
12.5	Optimization Method	575
	References	578
Appendix A.	Important Properties of Silicon, Silicon Dioxide and Silicon Nitride at 300 K	580
Appendix B.	Some Important Physical Constants at 300 K	581
Appendix C.	Unit Conversion Factors	581
Appendix D.	Magnitude Prefixes	581
Appendix E.	Methods of Calculating $\phi_s$ from the Implicit Eq. (6.23) or (6.30)	
Appendix F.	Charge Based MOSFET Intrinsic Capacitances	583
Appendix G.	Linear Regression	587
Appendix H.	Basic Statistical and Probability Theory	588
Appendix I.	List of Widely Used Statistical Package Programs	599
	Subject Index	600