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## SESSION 1 SUNDAY EVENING

Golden West

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7:00 **NEW HARDWARE PRODUCTS**  
H.L. Scalf, Chairman

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## SESSION 2 SUNDAY EVENING

California

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7:00 **NEW HARDWARE AND SOFTWARE PRODUCTS**  
D. Perkins, Chairman

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## SESSION 3 MONDAY MORNING

Presidio

PAPER #

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8:00 **WELCOME/OPENING REMARKS**

D. Brown, General Chairman  
J. Lipman, Conference Chairman

8:20 **CICC '91—TECHNICAL PROGRAM**

G. Ledenbach, Technical Program Committee Chairman

8:30 **KEYNOTE ADDRESS**

**Global Communications in the 1990's and the Impact on ASICs**

J.S. Mayo, Senior VP of Network Systems and Network Services, AT&T Bell Laboratories

9:30 **SONET/ATM**

Chairman: R. Cordell  
Co-Chairman: K. Huscroft

9:35 **INVITED**

**ASIC Technology Applied to SONET Multiplex, Transmission, and Cross-Connect Equipment**

M.A. McDonald, Rockwell International NTSD, Dallas, TX

3.1

10:00 **A SONET STS-3c User Network IC**

T.J. Robe and K.A. Walsh, Bellcore, Red Bank, NJ

3.2

10:25 **A 0.8- $\mu$ m BiCMOS Sea-of-Gates Implementation of the Tandem Banyan Fast Packet Switch**

F.M. Chiussi and F.A. Tobagi, Stanford University, Stanford, CA; and H. Amano, Keio University, Yokohama, Japan

3.3

10:50 **A Multi-Speed Digital Cross-Connect Switching VLSI Using New Circuit Techniques in Dual Port RAMs**

S. Shinagawa, Hitachi VLSI, Eng. Co., Ltd., Tokyo, Japan; and Y. Satoh, M. Mizukami, Y. Sonobe, Y. Nakano and T. Kanno, Hitachi Ltd., Japan

3.4

11:15 **1 GHz CMOS 12 : 1 Time Division MUX/DEMUX Pair**

K.R. Shastri and W.E. Carter, AT&T Bell Labs., Allentown, PA

3.5

11:40 **A LSI Chip Set for 2.4 Gb/s Fiber Optic Transmission**

S. Hatakeyama, T. Isogai, C. Konishi, M. Yagyu, N. Watanabe and K. Takahashi, NEC Corp., Kawasaki, Japan

3.6

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<b>SESSION 4</b>	<b>Friars/Padre/Sierra</b>	<b>PAPER #</b>
<b>MONDAY MORNING</b>		
<b>9:30 RELIABILITY SIMULATION AND MODELING</b> Chairman: C. Zukowski Co-Chairman: S. Cravens		
<b>9:35 TUTORIAL</b> <b>IC Reliability Simulation</b> C. Hu, University of California, Berkeley, CA		<b>4.1</b>
<b>10:25 Integrated Circuit Reliability Simulation Including Dynamic Stress Effects</b> W-J. Hsu, S.M. Gowda and B.J. Sheu, University of Southern California, Los Angeles, CA; and C-G. Hwang, Samsung Electronics, Yong In-Gun, Korea		<b>4.2</b>
<b>10:50 DYNAMO: A Program for the Simulation of Transient Faults in Digital Circuits</b> F.L. Yang and R.A. Saleh, University of Illinois, Urbana, IL		<b>4.3</b>
<b>11:15 A System for Electromigration Analysis in VLSI Metal Patterns</b> I.N. Hajj, V.B. Rao, R. Iimura, H. Cha and R. Burch, University of Illinois, Urbana, IL		<b>4.4</b>
<b>11:40 Design Model for Minority-Carrier Well-Type Guard Rings in CMOS Circuits</b> M.J. Chen, C.Y. Huang and C.Y. Wu, National Chiao-Tung University, Hsin-Chu, Taiwan; and P.N. Tseng and N.S. Tsai, Taiwan Semiconductor Mfg. Co. Ltd., Hsin-Chu, Taiwan		<b>4.5</b>
<b>12:05 LATE NEWS PAPER</b> <b>Mixed Mode Simulation of Slow Transient Effects in AlGaAs/GaAs HEMT Inverters</b> T. Wang and S-J. Wu, National Chiao-Tung University, Hsin-Chu, Taiwan		<b>4.6</b>

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<b>SESSION 5</b>	<b>Golden West</b>	<b>PAPER #</b>
<b>MONDAY MORNING</b>		
<b>9:30 ANALOG DESIGN AUTOMATION</b> Chairman: T. Sideris Co-Chairman: J. Lipman		
<b>9:35 A Design Tool for Weakly Nonlinear Analog Integrated Circuits with Multiple Inputs (Mixers, Multipliers)</b> P. Wambacq, J. Vanthienen, G. Gielen and W. Sansen, Katholieke Univ. Leuven, Heverlee, Belgium		<b>5.1</b>
<b>10:00 SEAS: A Simulated Evolution Approach for Analog Circuit Synthesis</b> Z-Q. Ning, T. Moutaana and H. Wallinga, Twente University, Enschede, The Netherlands		<b>5.2</b>
<b>10:25 HECTOR: A Hierarchical Topology-Construction Program for Analog Circuits Based on a Declarative Approach to Circuit Modeling</b> K. Swings, S. Donnay and W. Sansen, Katholieke Univ. Leuven, Heverlee, Belgium		<b>5.3</b>
<b>10:50 DAVE: An Automated Mixed Analog/Digital IC Layout Compiler</b> Z-M. Lin, University of Maryland, College Park, MD		<b>5.4</b>
<b>11:15 192 Automatic Custom Layout of Analog ICs Using Constraint-Based Module Generation</b> D.J. Chen and B.J. Sheu, University of Southern California, Los Angeles, CA		
<b>11:40 Fast Prototyping of Semi-Custom Bipolar Analog ASICs</b> Q. Buset, M. Declercq and F. Rahali, Swiss Federal Institute of Technology, Lausanne, Switzerland; and P. Vaucher, ASCOM Microelectronics, Bevaix, Switzerland		<b>5.6</b>

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## SESSION 6

MONDAY MORNING

California

PAPER #

- 9:30 **FPGA ARCHITECTURE AND APPLICATIONS**  
Chairman: C. McCarthy  
Co-Chairman: W. Carter
- 9:35 **Optimization of Field-Programmable Gate Array Logic Block Architecture for Speed** 6.1  
S. Singh, J. Rose, D. Lewis, K. Chung and P. Chow, University of Toronto, Toronto, Canada
- 10:00 **FPGA Performance vs. Cell Granularity** 6.2  
J.L. Kouloheris and A. El Gamal, Stanford University, Stanford, CA
- 10:25 **A High-Speed BiCMOS Table Look-Up Gate** 6.3  
P. Baltus, P. van der Meulen and M. Ligthart, Philips Research, Sunnyvale, CA
- 10:50 **A Large Scale FPGA with 10K Core Cells with CMOS 0.8  $\mu$ m 3-Layered Metal Process** 6.4  
H. Muroga, H. Murata, Y. Saeki, T. Hibi and Y. Ohashi, Semiconductor System Eng. Center., Kawasaki, Japan; and  
T. Noguchi and T. Nishimura, Microelectronics Center, Kawasaki, Japan
- 11:15 **GANGLION—A Fast Hardware Implementation of a Connectionist Classifier** 6.5  
C.E. Cox and W.E. Blanz, IBM Almaden Research Center, San Jose, CA
- 11:40 **Field Programmable Gate Array Key to Reconfigurable Array Outperforming Supercomputers** 6.6  
T. Waugh, Xilinx, Inc., San Jose, CA
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## SESSION 7

MONDAY AFTERNOON

Presidio

PAPER #

- 2:00 **HIGH SPEED TRANSCEIVERS AND DIGITAL CELLULAR MOBILE RADIO CIRCUITS**  
Chairman: D. Brown  
Co-Chairman: C. Jungo
- 2:05 **An Error-Correcting Encoder and Decoder for a 1 Gbit/s Fiber Optic Link** 7.1  
C. Benz, M. Gowan and K. Springer, Digital Equipment Corp., Hudson, MA
- 2:30 **A 60-MHz 64-Tap Echo Cancellor/Decision-Feedback Equalizer in 1.2  $\mu$ m CMOS for 281Q High Bit-Rate Digital Subscriber Line Transceivers** 7.2  
H. Samuelli, R.B. Joshi, B.C. Wong, B. Daneshrad, L.K. Tan, D. Kruse and H.T. Nicholas, University of California, Los Angeles, CA
- 2:55 **10 MB/S Twisted Pair CMOS Transceiver with Transmit Waveform Pre-equalization** 7.3  
C-C. Shih, J. Heideman, H. Shafir and S. Wurster, Level One Communications, Folsom, CA
- 3:20 **A Direct Sequence BPSK Spread Spectrum Transceiver Chip Set** 7.4  
C. Chien, L. Lau, G. Chen, B-Y. Chung, P.T. Yang, E. Cohen, H. Samuelli and R. Jain, University of California, Los Angeles, CA
- 3:45 **An Experimental TDMA Modulation/Demodulation CMOS VLSI Chip-Set** 7.5  
N.R. Sollenberger, Bellcore, Red Bank, NJ
- 4:10 **Integrated Digital Modulator and Analog Front-End for GSM Digital Cellular Mobile Radio System** 7.6  
B. Baggini, L. Coppero, G. Gazzoli and L. Sforzini, ITALTEL Sit, Milano, Italy; and F. Maloberti and G. Palmisano, Univ. di Pavia, Pavia, Italy
- 4:35 **LATE NEWS PAPER** 7.7  
**An Integrated Si Bipolar RF Transceiver for a Zero IF 900 MHz GSM Digital Mobile Radio Frontend of a Hand Portable Phone**  
J. Sevenhans and J. Wenin, Alcatel Bell, Antwerp, Belgium; and A. Vanwelsenaers and J. Baro, Alcatel Radio Telephone, Colombes, France

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- 4:50 **LATE NEWS PAPER** 7.8  
**A Power Efficient Channel Coder/Decoder Chip for GSM Terminals**  
H.J. Busschaert and P.P. Reusens, Alcatel Bell Telephone, Antwerp, Belgium; and L. Dartois and L. Desperben, Alcatel Thompson Radio Tel., Colombes, France
- 

## SESSION 8 MONDAY AFTERNOON

Friars/Padre Sierra

PAPER #

- 2:00 **CIRCUIT ANALYSIS AND SIMULATION**  
Chairman: R. Saleh  
Co-Chairman: B. Sheu
- 2:05 **Improving DC Convergence in a Circuit Simulator Using a Homotopy Method** 8.1  
L. Trajkovic, Bellcore, Morristown, NJ; and R.C. Melville and S-C. Fang, AT&T Bell Labs., Murray Hill, NJ
- 2:30 **Reversible Functional Simulation for Digital System Design** 8.2  
G. Jennings, Lund Univ., Lund, Sweden
- 2:55 **Calculation of a Total Dynamic Current of VLSI Using a Switch Level Timing Simulator (RSIM-FX)** 8.3  
N. Kimura and J. Tsujimoto, Toshiba Corp., Kawasaki, Japan
- 3:20 **Calculation and Application of Time Domain Waveform Sensitivities in Asymptotic Waveform Evaluation** 8.4  
A. Balivada, D.R. Holberg and L.T. Pillage, University of Texas, Austin, TX
- 3:45 **Static Charge Decay Analysis of MOS Circuits** 8.5  
G. Bischoff and R. Razdan, Digital Equipment Corp., Hudson, MA
- 4:10 **An Analytical-Model Generator for Interconnect Capacitances** 8.6  
U. Choudhury and A. Sangiovanni-Vincentelli, University of California, Berkeley, CA
- 4:35 **Modelling Behaviour and Tolerances in Analogue Cells** 8.7  
T. Koskinen and P.Y.K. Cheung, Imperial College, London, England
- 5:00 **Fast Simulated Diffusion: An Optimization Algorithm for Multi-Minimum Problems and Its Application to MOSFET Model Parameter Extraction** 8.8  
T. Sakurai and M. Ichida, Toshiba Corp., Kawasaki, Japan; and A.R. Newton, Univ. of California, Berkeley, CA
- 

## SESSION 9 MONDAY AFTERNOON

Golden West

PAPER #

- 2:00 **FILTERS AND AMPLIFIERS**  
Chairman: A. Barlow  
Co-Chairman: A. Grebene
- 2:05 **A CMOS Wideband Amplifier with 800 MHz Gain-bandwidth** 9.1  
F. Op't Eynde, Mietec Alcatel, Brussels, Belgium; and W. Sansen, Katholieke Univ. Leuven, Heverlee, Belgium
- 2:30 **A CMOS Biquad at VHF** 9.2  
M. Snelgrove and A. Shoval, Univ. of Toronto, Toronto, Canada
- 2:55 **An Adaptive Analog Continuous-Time CMOS Biquadratic Filter** 9.3  
T. Kwan and K. Martin, UCLA, Los Angeles, CA
- 3:20 **A 50 MHz Variable Gain Amplifier Cell in 2  $\mu$ m CMOS** 9.4  
R. Gomez and A.A. Abidi, Univ. of California, Los Angeles, CA

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- 3:45 **2—10 MHz Programmable Continuous-Time .05 Degree Equiripple Linear Phase Filter** 9.5  
G.A. DeVairman and R.G. Yamasaki, Silicon Systems, Inc., Tustin, CA
- 4:10 **A 32Mb/s Disk Drive Data Separator for Constant Density Recording** 9.6  
R. Horita, S. Miyazawa, K. Hase, A Hirano and S. Kojima, Hitachi Ltd., Yokohama City, Japan
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## SESSION 10

### MONDAY AFTERNOON

### California

### PAPER #

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#### 2:00 SPECIALTY RAMS AND APPLICATIONS

Chairman: K. Venkateswaran  
Co-Chairman: K. Au

- 2:05 **A 50-MHz 10ns Submicron BiCMOS 2-Way Set Associative Cache TAG Memory** 10.1  
E.H. Chiu and Q.D. An, Texas Instruments, Dallas, TX
- 2:30 **2.6 Gbyte/sec Bandwidth Cache/TLB Macro for High-Performance RISC Processor** 10.2  
T. Takayangi, K. Sawada, M. Takahashi, Y. Ito, Y. Toyoshima, H. Hayashida and M. Norishima, Toshiba Corp., Kawasaki, Japan; and M. Uchida, Toshiba Microelectronics Corp., Japan
- 2:55 **A 288-kbit Fully Parallel Content Addressable Memory Using Stacked Capacitor Cell Structure** 10.3  
T. Yamagata, M. Mihara, T. Hamamoto, T. Kobayashi and M. Yamada, Mitsubishi Electric Corp., Itami, Japan
- 3:20 **“New Bit Line Architecture for Ultra High Speed SRAMs”—T-Shaped Bit Line and It’s Real Application to 256 K BiCMOS TTL SRAM** 10.4  
T. Shiomi, T. Wada, S. Ohbayashi, A. Ohba, H. Honda, Y. Ishigaki, M. Hatanaka, S. Nagao, K. Anami and T. Sumi, Mitsubishi Electric Corp., Itami, Japan
- 3:45 **A CMOS 4 ch × 1k Time Memory LSI with 1 ns Resolution** 10.5  
Y. Arai, KEK, National Lab for High Energy Physics, Ibaraki, Japan; and T. Matsumura and K. Endo, NTT, Atsugi-shi, Japan
- 4:10 **Implementation of Sub-10ns Serial Access Mode to a Standard 64-Mb DRAM** 10.6  
Y. Watanabe, K. Tsuchida, Y. Oowaki, D. Takashima, M. Ohta, H. Nakano, S. Watanabe and K. Ohuchi, Toshiba Corp., Kawasaki, Japan
- 4:35 **A High Speed Memory System Based on 16 Mb ST (Stretchable Memory Matrix) DRAMs** 10.7  
T. Ooishi, M. Asakura, H. Hidaka, K. Arimoto and K. Fujishima, Mitsubishi Electric Corp., Itami, Japan
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## SESSION 11

### TUESDAY MORNING

### Presidio

### PAPER #

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#### 8:30 SYNTHESIS AND VERIFICATION

Chairman: M. Tarsi  
Co-Chairman: T. Sideris

- 8:35 **A Comparison of an ASIC Synthesized Design to a Schematic Entry Design for a Viterbi Decoder** 11.1  
C.A. Gray and M.J.S. Smith, Univ. of Hawaii, Honolulu, HI; J. Rowson and M. O'Brien, VLSI Technology, Inc., San Jose, CA
- 9:00 **New State Assignment Algorithms for Finite State Machines Using Look Ahead** 11.2  
J.J. Yang, H. Shin and J.W. Chong, HanYang Univ., Seoul, Korea
- 9:25 **Improving BDDs Manipulation Through Incremental Reduction and Enhanced Heuristics** 11.3  
N. Calazans, R. Jacobi, Q. Zhang and C. Trullemans, Universite Catholique de Louvain, Louvain-la-Neuve, Belgium

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9:50	<b>A System for Synthesis of Sequential Machines with Built-In Testability</b>	11.4
	B. Mitra, Texas Instruments (India) Pvt. Ltd., Bangalore, India; and S. Misra and P. Pal Choudhuri, Indian Institute of Technology, Kharagpur, India	
10:15	<b>Symbolic Verification of CMOS Synchronous Circuits Using Characteristic Functions</b>	11.5
	Y. Kukimoto and H. Tanaka, Univ. of Tokyo, Tokyo, Japan; and M. Fujita, Fujitsu Labs., Kawasaki, Japan	
10:40	<b>Optimal Synthesis of High Performance Architectures</b>	11.6
	C.H. Gebotys and M.I. Elmasry, University of Waterloo, Waterloo, Canada	
11:05	<b>LATE NEWS PAPER</b>	11.7
	<b>Memory Synthesis for High Speed DSP Applications</b>	
	P.E.R. Lippens, J. Meerberger, A. van der Werf, W.F.J. Verhaegh, B.T. McSweeney, Philips Research Labs., Eindhoven, The Netherlands	

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## SESSION 12 TUESDAY MORNING

Friars/Padre/Sierra

PAPER #

8:30	<b>REAL-TIME IMAGE PROCESSING &amp; COMPRESSION</b>	
	Chairman: P. Ivey Co-Chairman: L. D'Luna	
8:35	<b>A Single Chip Sensor &amp; Image Processor for Fingerprint Verification</b>	12.1
	S. Anderson, W.H. Bruce, P.B. Denyer, D. Renshaw and G. Wang, Univ. of Edinburgh, Edinburgh, Scotland	
9:00	<b>A Complete Single-Chip Implementation of the JPEG Image Compression Standard</b>	12.2
	M. Bolton, SGS-Thomson Microelectronics, Bristol, U.K.	
9:25	<b>A 50 MHz Vision Processor</b>	12.3
	J. Fandrianto, B. Martin, H. Rainnie, S. Sutardja and C-S. Wang, Integrated Information Technology, Santa Clara, CA	
9:50	<b>A Data-Flow Processor for Real-Time Low-Level Image Processing</b>	12.4
	G.M. Quenot and B. Zavidovique, DGA/Etablis, Technique Central de l'Armement, Arcueil, France	
10:15	<b>A 180-Mbps Lossless Video Compression Chip</b>	12.5
	W-C. Fang and B. J. Shell, Univ. of Southern California, Los Angeles, CA; and R. Nixon, C.I.T. Jet Propulsion Lab., Pasadena, CA	
10:40	<b>CCD Image Sensor with Differential, Pyramidal Output for Lossless Image Compression</b>	12.6
	S.E. Kemeny, H. Torby and H. Meadows, Columbia, Univ., New York, NY; E.R. Fossum, CalTech, Pasadena, CA; and R. Bredthauer and M. LaShell, Ford Aerospace, Newport Beach, CA	
11:05	<b>A Customizable Timing Controller for Electronic Imaging Applications</b>	12.7
	J.A. Vincent, W.A. Cook, L.J. D'Luna, G.W. Brown and R.M. Guidash, Eastman Kodak Company, Rochester, NY	

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## SESSION 13 TUESDAY MORNING

Golden West

PAPER #

8:30	<b>TEST I</b>	
	Chairman: S. Davidson Co-Chairman: P. Fasang	
8:35	<b>TUTORIAL</b>	13.1
	<b>CMOS IC Fault Models, Physical Defect Coverage and I<sub>DDQ</sub> Testing</b>	
	R.R. Fritzemeier and J.M. Soden, Sandia National Labs., Albuquerque, NM; and C.F. Hawkins, The Univ. of New Mexico, Albuquerque, NM	

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<b>9:25</b>	<b>Can IDDQ Test Replace Conventional Stuck-Fault Test?</b>	<b>13.2</b>
	D.M. Su, IBM Corp., Boca Raton, FL	
<b>9:50</b>	<b>A Comparison of Methods for Supply Current Analysis</b>	<b>13.3</b>
	J.F. Frenzel, Univ. of Idaho, Moscow, ID; and P.N. Marinos, Duke Univ., Durham, NC	
<b>10:15</b>	<b>Circuit Design for Built-In Current Testing</b>	<b>13.4</b>
	M. Patyra and W. Maly, Carnegie Mellon Univ., Pittsburgh, PA	
<b>10:40</b>	<b>A Framework for Design for Testability of Mixed Analog/Digital Circuits</b>	<b>13.5</b>
	M. Jarwala and S-J. Tsai, AT&T Bell Labs., Princeton, NJ	
<b>11:05</b>	<b>An Experimental Approach to Analog Fault Models</b>	<b>13.6</b>
	M. Soma, University of Washington, Seattle, WA	

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## SESSION 14 TUESDAY MORNING

## California

## PAPER #

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<b>8:30</b>	<b>HIGH PERFORMANCE GATE ARRAYS</b>	
	Chairman: G. Sporzynski Co-Chairman: R. Blake	
<b>8:35</b>	<b>Can CMOS Resist the BiCMOS Challenge?</b>	<b>14.1</b>
	L. Wissel and E. Gould, IBM General Technology Division, Essex Junction, VT	
<b>9:00</b>	<b>Strategies for CMOS/BiCMOS Gate Usage on Sea-of-Gates Arrays</b>	<b>14.2</b>
	P.P. Duchene and M.J. Declercq, Swiss Fed. Inst. of Technology, Lausanne, Switzerland	
<b>9:25</b>	<b>A 1.9ns BiCMOS CAM Macro with Double Match Line Architecture</b>	<b>14.3</b>
	T. Nagamatsu, T. Sakurai, H. Hara, S. Kobayashi, K. Seta and M. Noda, Toshiba Corp., Kawasaki, Japan; M. Uchida, Y. Watanabe and F. Sano, Toshiba Microelectronics Corp., Japan	
<b>9:50</b>	<b>0.5 <math>\mu</math>m BiCMOS SOG with Selectable 5v/3.3v Operations</b>	<b>14.4</b>
	Y. Tanaka, T. Sei, S. Ishimoto and T. Kobayashi, Toshiba Corp., Kawasaki, Japan; M. Ishibashi and A. Kurahara, Toshiba Microelectronics Corp., Japan	
<b>10:15</b>	<b>A BiCMOS Circuit Family for a 0.45 <math>\mu</math>m CMOS/BiCMOS Sea-of-Gates</b>	<b>14.5</b>
	G. Boudon, D. Plassat, R. Cullet, R. Trauet and D. Mauchauffee, IBM France, Corbeil-Essonnes, France	
<b>10:40</b>	<b>A Quasi-Complementary-Logic GaAs Gate Array Employing Air-Bridge Metalization Technology</b>	<b>14.6</b>
	N. Higashisaka, M. Shimada, T. Nishimura, N. Sasaki, M. Noda, H. Matsuoka and S. Kayano, Mitsubishi Electric Corp., Itami, Japan	
<b>11:05</b>	<b>A High-Density GaAs Gate Array Architecture</b>	<b>14.7</b>
	G. Lee, B. Donckels, A. Grey and I. Deyhimy, Vitesse Semiconductor Corp., Camarillo, CA	

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## SESSION 15 TUESDAY MORNING

Presidio

PAPER #

### 2:00 ADVANCES IN DATA PROCESSING ELEMENTS

Chairman: S. Law  
Co-Chairman: Y. Horiba

### 2:05 A 120 MFLOP CMOS Floating Point Processor

P. Chai, T. Chuk, Y.H. Fong, L. Hu, K. Ng, J. Prabhu, A. Quek, A. Samuels and J. Youn, Weitek Corp., Sunnyvale, CA

15.1

### 2:30 A 80 MFLOPS 64-Bit Microprocessor for Parallel Computer

H. Nakano, M. Nakajima, Y. Nakakura, T. Yoshida, Y. Goi, Y. Nakai, R. Segawa, T. Kishida and H. Kadota, Matsushita Electric Industrial Co. Ltd., Osaka, Japan

15.2

### 2:55 A 1.5 MLIPS 40-bit AI Processor

H. Machida, H. Ando, C. Ikenaga, H. Nakashima, A. Maeda and M. Nakaya, Mitsubishi Electric Corp., Itami, Japan

15.3

### 3:20 A Two-Chip CMOS 64b Mainframe Processor Chipset

M. Yamagishi and K. Koide, Hitachi, Ltd., Tokyo, Japan; A. Ishiyama, A. Yamagiwa and T. Hayashi, Hitachi Ltd., Japan; and Y. Satou, Hitachi VLSI Engineering Co., Ltd., Tokyo, Japan

15.4

### 3:45 Memory Chip for 24-Port Global Register File

W. Maly, M. Patyra, A. Primatic, V. Raghavan, T. Storey and A. Wolfe, Carnegie Mellon Univ., Pittsburgh, PA

15.5

### 4:10 A 64b CMOS Mainframe Execution Unit Macrocell with Error Detecting Circuit

T. Hayashi, T. Doi, M. Yamagishi, K. Koide, A. Ishiyama and M. Hiramatsu, Hitachi Ltd., Tokyo, Japan; and A. Yamagiwa, Kanagawa Works, Kanagawa, Japan

15.6

### 4:35 LATE NEWS PAPER

#### High Performance Self-Checking Adder for VLSI Processor

F-H.W. Shih, IBM Corp., Yorktown Heights, NY

15.7

### 4:50 LATE NEWS PAPER

#### 3.3-V BiCMOS Circuit Techniques for 250-MHz RISC Arithmetic Modules

K. Yano, M. Hiraki, S. Shukuri, M. Hanawa, M. Suzuki, T. Nishida and K. Seki, Hitachi Central Research Lab., Tokyo, Japan; and S. Morita, A. Kawamata and N. Ohki, Hitachi VLSI Eng. Corp., Tokyo, Japan

15.8

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## SESSION 16 TUESDAY AFTERNOON

Friars/Padre/Sierra

PAPER #

### 2:00 NEURAL NETWORKS AND GRAPHICS PROCESSORS

Chairman: F. Yassa  
Co-Chairman: J. Barnes

### 2:05 A Trainable Analog Neural Chip for Image Compression

C-F. Chang, B.J. Sheu, W-C. Fang and J. Choi, University of Southern California, Los Angeles, CA

16.1

### 2:30 A BiCMOS Image Sensor with a Chopper-Stabilized Edge Detector & a Correlated-Double-Sampling Readout Circuit for Neural Network VLSI Operating at 77K

T.L. Chou, E.J. Wong, W.C. Lee and J.B. Kuo, National Taiwan Univ., Taipei, Taiwan

16.2

### 2:55 A High Performance Digital Processor for Implementing Large Artificial Neural Networks

D.A. Orrey, D.J. Myers and J.M. Vincent, British Telecom Martlesham Heath, U.K.

16.3

### 3:20 A Vector Digital Signal Processor LSI for Speaker-Independent Voice Pattern Matching

N. Matsubishi, Y. Tokuno, M. Mizutani, T. Uehara and H. Ando, OKI Electric Industry Co., Ltd., Tokyo, Japan

16.4



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3:45	<b>100M pixel/sec Single-Chip Integrated Graphics Controller (ICG)</b>	16.5
	D. Mansharamani, M. Birman, G. Chu, J. Martinella, D. Wu, J. Chiou, B. Wallis, M. Zhu, K. Evans, J. McLeod, H. Grewal, K. Goodin and A. Samuels, Weitek Corp., Sunnyvale, CA	
4:10	<b>A 170MHz CMOS Pixel Processor for Windowing Graphics</b>	16.6
	W.N. Schnaitter, S.L. Urmston and A. Pon, Brooktree Corp., San Diego, CA	
4:35	<b>LATE NEWS PAPER</b>	16.7
	<b>Digital Logarithmic CMOS Multiplier for Very-High-Speed Signal Processing</b>	
	F. Hoefflinger, M. Selzer and F. Warkowski, Institut fur Mikroelektronik, Stuggart, Germany	

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## SESSION 17 TUESDAY AFTERNOON

### Golden West

### PAPER #

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2:00	<b>TEST II</b>	
	Chairman: S. Runner Co-Chairman: P. Fasang	
2:05	<b>The Architecture of the GenTest Sequential Test Generator</b>	17.1
	R. Bencivenga, T.J. Chakraborty and S. Davidson, AT&T Bell Labs., Princeton, NJ	
2:30	<b>Test Considerations for BiCMOS Logic Families</b>	17.2
	K. Roy, Texas Instruments, Inc., Dallas, TX; M.E. Levitt, Sun Microsystems, Mt. View, CA; and J.A. Abraham, Univ. of Texas, Austin, TX	
2:55	<b>PASCANT: A Partial Scan and Test Generation System</b>	17.3
	S. Bhawmik and C.J. Lin, AT&T Bell Labs., Princeton, NJ; and K.T. Cheng and V.D. Agrawal, AT&T Bell Labs., Murray Hill, NJ	
3:20	<b>Accurate Modeling and Simulation of Bridging Faults</b>	17.4
	J.M. Acken, Intel Corp., Santa Clara, CA; and S.D. Millman, Motorola, Inc., Tempe, AZ	
3:45	<b>Application of Boundary-Scan and Full-Chip BIST to a 3 ASIC Chip Set</b>	17.5
	K.D. Fitch and J. Kane, AT&T Bell Labs., Allentown, PA	
4:10	<b>Current Bias Testing of Differential Circuits</b>	17.6
	P. Phillips, K. Patel, J. Monzel, W. Reohr, C. Beh and C. Radke, IBM General Technology Div., Hopewell Junction, NY	
4:35	<b>LATE NEWS PAPER</b>	17.7
	<b>On Applying Circular Self-Test Path (CSTP) Technique to Circuits</b>	
	C.A. Njinda, R. Srinivasan and M.A. Breuer, Univ. of Southern California, Los Angeles, CA	

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## SESSION 18 TUESDAY AFTERNOON

### California

### PAPER #

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2:00	<b>FABRICATION TECHNOLOGY</b>	
	Chairman: R. Kumar Co-Chairman: D. Wayne	
2:05	<b>A Bonded-SOI-Wafer CMOS 16 Bit 50KSPS Delta-Sigma ADC</b>	18.1
	T. Takaramoto, S.S. Harajiri, O. Kobayashi and K. Gotoh, Fujitsu Ltd., Kawasaki, Japan; and M. Sawada, Fujitsu VLSI Ltd., Nagoya, Japan	
2:30	<b>A Novel Three Dimensional BiCMOS Process Using Epitaxial Lateral Overgrowth of Silicon</b>	18.2
	R. Bashir, S. Venkatesan and G.W. Neudeck, Purdue University, W. Lafayette, IN	

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- 2:55 A 3.3V, 0.5  $\mu$ m BiCMOS Technology for BiNMOS and ECL Gate** 18.3  
H. Miyakawa, M. Norishima, Y. Niitsu, H. Momose and K. Maeguchi, Toshiba Corp., Kawasaki, Japan
- 3:20 Submicron C BiCMOS Technology with New Well and Buried Layer Formed by Multiple Energy Ion Implementation** 18.4  
K. Higashitani, T. Kuroi, K. Suda, M. Hatanaka, S. Nagao and N. Tsubouchi, Mitsubishi Electric Corp., Itami, Japan
- 3:45 Field-Plated High Gain Lateral Bipolar Transistor in Standard CMOS Process for BiNMOS Application** 18.5  
K.K. Au, K.K. Diogu, P.G.Y. Tsui, M.L. Kosty, C.M. Palmer and Y.S. Kim, Motorola, Inc., Austin, TX
- 4:10 A Modular Memory and Process Verification Vehicle for a Sub-Micron BiCMOS Telecom Technology** 18.6  
K.J. Schultz, G.F.R. Gibson, A.L. Silburt, R.G. Gibbins and N. Mehta, Bell-Northern Research Ltd., Ottawa, Canada; and R.S. Phillips, Bayview Technologies, Inc., Constance Bay, Canada
- 4:35 A Modular Flash EEPROM Technology for 0.8  $\mu$ m High Speed Logic Circuits** 18.7  
K-M. Chang, S. Cheng and C. Kuo, Motorola, Inc., Austin, TX
- 5:00 Performance and Technology Trade-Offs of BiCMOS Submicron Processes for ASIC Applications** 18.8  
L. Gal, C. Prunty and R. Kumar, Unisys Corp., San Diego, CA
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## SESSION 19 TUESDAY EVENING

Friars/Padre/Sierra

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- 8:00 EVENING PANEL**  
**MANAGING ASIC PROFITABILITY IN THE 1990's**  
Moderator: R. Kumar, Unisys Corporation
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## SESSION 20 TUESDAY EVENING

Golden West

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- 8:00 EVENING PANEL**  
**2001—A SYNTHESIS ODYSSEY**  
Moderator: J. Lipman, VLSI Technology, Inc.
- 

## SESSION 21 TUESDAY EVENING

California

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- 8:00 EVENING PANEL**  
**MIXED SIGNAL TEST DEVELOPMENT: THE FINAL FRONTIER?**  
Moderator: H.L. Scaff, Gould AMI Semiconductors
-

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## SESSION 22 WEDNESDAY MORNING

Presidio

PAPER #

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- 8:30 **COMPILER AND LIBRARY METHODOLOGY**  
Chairman: S. Mori  
Co-Chairman: J. Buurma
- 8:35 **ACAP—A System for the Interactive Graphical Capture of Module Generators** 22.1  
R.A. Eesley and M.A. Tarsi, Mentor Graphics Corp., Warren, NJ
- 9:00 **Device Sizing for Silicon Compilers Using CSL** 22.2  
L.T. Walczowski, M.H. Smith, W.A.J. Waller and D. Howard, Univ. of Kent, Canterbury, U.K.
- 9:25 **A Sub-Micron CMOS Embedded SRAM Compiler** 22.3  
J. Tou and P. Gee, Motorola, Inc., Chandler, AZ; and J. Duh and R. Eesley, Mentor Graphics Corp., Warren, NJ
- 9:50 **A Dual-Port SRAM Compiler for 0.8 Micron 100K BiCMOS Gate Arrays** 22.4  
T. Dao and F. Svejda, Texas Instruments Inc., Dallas, TX
- 10:15 **A Procedural DATAPATH Compiler for VLSI Full Custom Applications** 22.5  
M. Taliercio and G. Foletto, SGS Thomson Microelectronics, Agrate Brianza, Italy; and L. Licciardi, CSELT, Torino, Italy
- 10:40 **Automated Generation of Custom Pad Cells for ASICs** 22.6  
M. Braiman and J. Kuppinger, NCR Microelectronics, Fort Collins, CO
- 11:05 **Exploiting 0.8-Micron ASIC Libraries from Different Vendors** 22.7  
A. Kurosawa, VLSI Technology, Inc., San Jose, CA; and S. Shimada, Hitachi Ltd., Tokyo, Japan
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## SESSION 23 WEDNESDAY MORNING

Friars/Padre/Sierra

PAPER #

- 
- 8:30 **DEVICE AND PROCESS MODELING AND SIMULATION**  
Chairman: P. Zeitzoff  
Co-Chairman: R. Milano
- 8:35 **INVITED TUTORIAL** 23.1  
**The Use of TCAD in Semiconductor Technology Development**  
E. Buturla, IBM Corp., Essex Junction, VT
- 9:25 **An Accurate MOS Transistor Model for Submicron VLSI Circuits—BSIM<sub>plus</sub>** 23.2  
S.M. Gowda and B.J. Sheu, Univ. of Southern California, Los Angeles, CA; and J.S. Cable, TRW, Inc., Redondo Beach, CA
- 9:50 **A New Large Signal Model for Heterojunction Bipolar Transistors Including Temperature Effects** 23.3  
P. Baureis, W. McKinley and D. Seitzer, Fraunhofer-Inst. for Integrated Circuits, Erlangen, Germany
- 10:15 **Device-Level Analysis of a 1  $\mu$ m BiCMOS Inverter Circuit Operating at 77K Using a Modified PISCES Program** 23.4  
J.B. Kuo, Y.W. Chen and K.H. Lou, National Taiwan University, Taipei, Taiwan
- 10:40 **High-Frequency Characterization and Modeling of Polysilicon and Diffusion Lines** 23.5  
W.R. Eisenstadt and O. Bell, University of Florida, Gainesville, FL
- 11:05 **A Tool Towards Integration of IC Process, Device, and Circuit Simulation** 23.6  
G. Chin, Z. Yu and R.W. Dutton, Stanford University, Stanford, CA
- 11:30 **LATE NEWS PAPER** 23.7  
**A Pragmatic Approach to Integrated Process/Device/Circuit Simulation for IC Technology Development**  
K.R. Green and J.G. Fossum, Univ. of Florida, Gainesville, FL
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## SESSION 24 WEDNESDAY MORNING

Golden West

PAPER #

- 8:30 ANALOG CIRCUIT APPLICATIONS**  
Chairman: D. Lynch  
Co-Chairman: D. Embree
- 8:35 Fully-Differential CMOS Current-Mode Circuits** 24.1  
R.H. Zele and D.J. Allstot, Carnegie Mellon University, Pittsburgh, PA; and T.S. Fiez, Washington State University, Pullman, WA
- 9:00 A 14 Bit CMOS A/D Converter Based on Dynamic Current Memories** 24.2  
P. Deval and M.J. Declercq, Swiss Fed. Inst. of Technology, Lausanne, Switzerland; and J. Robert, TESTA, S.A., Renens, Switzerland
- 9:25 A Transistor-Only Current Mode  $\Sigma \Delta$  Modulator** 24.3  
S.J. Daubert, AT&T Bell Labs., Murray Hill, NJ; and D. Vallancourt, Columbia University, New York, NY
- 9:50 A Single-Chip Voiceband Signal Processor for Integrated Facsimile and Data Modems** 24.4  
D.J. Chen, W. Ngai, S. Taylor, D. Shum, F. In'tveld, G. Kinoshita and T. Kojima, Sharp Digital Information Products, Inc., Irvine, CA; and M. Uratani, H. Ogawa and S. Hattori, Sharp IC Group, Tenri, Japan
- 10:15 A 5-V CMOS Line Controller with 16-Bit Audio Converters** 24.5  
L. LeToumelin, P. Carbou, Y. Leduc and P. Guignon, Texas Instruments, Loubet, France; and J. Oredsson and A. Lindberg, Ericsson Components, Stockholm, Sweden
- 10:40 A Fully Integrated High Performance FM Stereo Decoder** 24.6  
G.J. Manlove, J.J. Marrah and R.A. Kennedy, Delco Electronics Corp., Kokomo, IN
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## SESSION 25 WEDNESDAY MORNING

California

PAPER #

- 8:30 HIGH-PERFORMANCE CIRCUITS AND CELL LIBRARY DEVELOPMENT**  
Chairman: M. Mittal  
Co-Chairman: R. Bryant
- 8:35 Dynamic Asynchronous Logic for High Speed CMOS Systems** 25.1  
A. McAuley, Bellcore, Morristown, NJ
- 9:00 Current-Mode Logic Techniques for CMOS Mixed-Mode ASIC's** 25.2  
D.J. Allstot, Carnegie Mellon University, Pittsburgh, PA; G. Liang, Exar Corp., San Jose, CA; and H.C. Yang, National Semiconductor Inc., Santa Clara, CA
- 9:25 A 700-MHz 24-Bit Pipelined Accumulator in 1.2  $\mu\text{m}$  CMOS for Application as a Numerically Controlled Oscillator** 25.3  
F. Lu and H. Samuelli, Univ. of California, Los Angeles, CA; and J Yuan and C. Svensson, Linkoping Univ., Linkoping, Sweden
- 9:50 A Knowledge Based Project Plan Generation and Control System for ASIC Design Management** 25.4  
K.D. Müller-Glaser, K. Neusinger and K. Kirsch, Univ. of Erlangen-Nurnberg, Erlangen-Tennenlohe, Germany
- 10:15 Technology-and Power-Supply-Independent Cell Library** 25.5  
J.M. Masgonty, C. Arm and C. Pigué, CSEM, Neuchatel, Switzerland
- 10:40 An Integrated Design and Characterization Environment for the Development of a Standard Cell Library** 25.6  
J.C. Herbert, Mentor Graphics Corp., Warren, NJ
- 11:05 LATE NEWS PAPER** 25.7  
**Characterizing a VLSI Standard Cell Library**  
M.A. Cirit, Adaptec Inc., Milpitas, CA
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## SESSION 26

WEDNESDAY AFTERNOON

Presidio

PAPER #

**1:30 DATA CONVERSION CIRCUITS**

Chairman: D. Allstot  
Co-Chairman: I. Scott

- 1:35 A 12-Bit Video BiCMOS Track-and-Hold Amplifier Using Analog Calibration** 26.1  
M. Nayebi, R. Schmitt, C. Yee and N. Bhandari, Vanguard Semiconductor, Milpitas, CA; and S. Yu and T. Batra, California Micro Devices, Tempe, AZ
- 2:00 A Rail-to-Rail Video-Band Full Nyquist 8-Bit A/D Converter** 26.2  
N. Shiwaku, Y. Tung, T. Hiroshima, K-S. Tan, T. Kurosawa, K. McDonald and M. Chiang, Texas Instruments, Inc., Dallas, TX
- 2:25 A CMOS 20MHz 8Bit 50mW ADC for Mixed Analog/Digital ASICs** 26.3  
K. Tsuji and H. Sugiyama, Toshiba Corp., Kawasaki, Japan; and N. Sugawa, Toshiba Microelectronics, Corp., Japan
- 2:50 A Pipelined 9-Stage Video-Rate Analog-to-Digital Converter** 26.4  
S.H. Lewis, H.S. Fetterman, G.F. Gross, Jr., R. Ramachandran and T.R. Viswanathan, AT&T Bell Labs., Reading,
- 3:15 A 10bit 80MHz Glitchless CMOS D/A Converter** 26.5  
H. Takakura, M. Yokoyama and A. Yamaguchi, Toshiba Corp., Kawasaki, Japan
- 3:40 A 10 Bit 75 Mega-Sample per Second A/D Converter** 26.6  
J. Marsh, K. Lofstrom, J. Engert and B. Price, Tektronix, Inc., Beaverton, OR
- 4:05 LATE NEWS PAPER** 26.7  
**A CMOS 9 bit 25 MHz 100mW ADC for Mixed Analog/Digital LSIs**  
M. Kasahara, K. Yahagi, H. Sonoda, S. Ueda and T. Matsuura, Hitachi, Ltd., Gunma, Japan

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## SESSION 27

WEDNESDAY AFTERNOON

Friars/Padre/Sierra

PAPER #

**1:30 PACKAGING AND INTERFACES**

Chairman: W. Vincent  
Co-Chairman: J. Tandon

- 1:35 INVITED** 27.1  
**Factors in Implementing MCM Solutions for the High Performance Systems of the 1990s**  
M.L. Buschbom, Texas Instruments, Dallas, TX; and S.E. Calvin, Sequent Computers, Beaverton, OR
- 2:00 A New On-Chip ESD Protection Circuit with Dual Parasitic SCR Structures for CMOS VLSI** 27.2  
C-Y. Wu and M-D. Ker, Natl. Chiao-Tung Univ., Hsin-Chu, Taiwan; C-Y. Lee, J. Ko and L. Lin, United Microelectronics Corp., Hsin-Chu, Taiwan
- 2:25 The Design of a Monolithic, Signal Conditioned Pressure Sensor** 27.3  
I. Baskett, R. Frank and E. Ramsland, Motorola, Inc., Phoenix, AZ
- 2:50 A Photodetector Array for a One Terabyte Optical Tape Recorder** 27.4  
P. Self and R. Miller, Avasem Corp., San Jose, CA; K. Brehmer, Exar Corp., San Jose, CA; and R. Bielak, CREO Products, Inc., Burnaby, Canada
- 3:15 1.2 Gb/s Integrated Laser Driver with Temperature Compensation for Modulation Current** 27.5  
K.R. Shastri and R.F. Benjamin, AT&T Bell Labs., Allentown, PA; J.J. Royer and K.A. Yanusheski, AT&T Solid State Tech. Center, Breinigsville, PA

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- 3:40 LATE NEWS PAPER** **27.6**  
**A 60V-10A Intelligent Power Switch Using Standard Cells**  
S.L. Wong, S. Venkatasubrahmanian, M.J. Kim and J.C. Young, Philips Labs., Briarcliff Manor, NY
- 3:55 LATE NEWS PAPER** **27.7**  
**VLSI Silicon-Based Prosthesis for In-Vitro Measurement of Neural Activity**  
K.J. Rambo, R.M. Fox, W.R. Eisenstadt, D.S. Langford and J. Principe, Univ. of Florida, Gainesville, FL; and R. Palovcik, Epilepsy Research Foundation of Florida
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## SESSION 28

### WEDNESDAY AFTERNOON

### Golden West

### PAPER #

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- 1:30 PLACEMENT AND ROUTING**  
Chairman: T. Yanagawa  
Co-Chairman: J. Lipman
- 1:35 Timing Driven Routing and Resistivity Minimization** **28.1**  
R. Hojati, Cadence Design Systems, Inc., Santa Clara, CA
- 2:00 An Efficient Eigenvector-Node Interchange Approach for Finding Netlist Partitions** **28.2**  
A. Vannelli, S.W. Hadley and B.L. Mark, Univ. of Waterloo, Waterloo, Canada
- 2:25 Cell-Shifting Compaction of Building-Cell Methodology for High-Speed GaAs Standard-Cell LSIs** **28.3**  
T. Sasaki, K. Kawakyu, T. Seshita, A. Kameyama, T. Terada, Y. Kitaura, K. Ishida and N. Uchitomi, Toshiba Corp., Kawasaki, Japan
- 2:50 Hybrid Routing on Multichip Modules** **28.4**  
C-C. Tsai, S-J. Chen and W-S. Feng, National Taiwan Univ., Taipei, Taiwan; and P.Y. Hsiao, National Chiao Tung University, Hsinchu, Taiwan
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## SESSION 29

### WEDNESDAY AFTERNOON

### California

### PAPER #

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- 1:30 QUALITY AND RELIABILITY**  
Chairman: S. Quigley  
Co-Chairman: S. Runner
- 1:35 INVITED** **29.1**  
**A Six Sigma Program Implementation**  
P.A. Tobias, IBM Corp., Hopewell Junction, NY
- 2:00 Analog Statistical Simulation** **29.2**  
M. Rencher, Motorola, Inc., Tempe, AZ
- 2:25 Hierarchical Simulation of Hot-Carrier Induced Damages in VLSI Circuits** **29.3**  
Y. Leblebici, P.C. Li, S.M. Kang and I.N. Hajj, University of Illinois, Urbana, IL
- 2:50 Metastability of CMOS Master/Slave Flip-Flops** **29.4**  
T.J. Gabara, AT&T Bell Labs., Allentown, PA; and G.J. Cyr and C.E. Stroud, AT&T Bell Labs., Naperville, IL
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