CONTENTS

Preface vii

PART ONE Specification and Design of Reactive Systems 1

1 Synchronous languages for hardware and software reactive systems
G. Berry 3

2 Towards a complete design method for embedded systems using Predicate/Transition-Nets
B. Kleinjohann, J. Tacken and C. Tahedl 4

PART TWO Verification Using Model Checking Techniques (+ Poster Abstracts) 25

3 Simplifying data operations for formal verification
F. Balarin and K. Sajid 27

4 CTL and equivalent sublanguages of CTL
K. Schneider 40

5 Verifying linear temporal properties of data intensive controllers using finite instantiations
R. Hojati, D. Dill and R.K. Brayton 60

6 A high-level language for programming complex temporal behaviors and its translation into synchronous circuits (poster abstract)
C.-T. Chou, J.-L. Huang and M. Fujita 74

7 System-level hardware design with μ-charts (poster abstract)
J. Philipps and P. Scholz 77

8 Interface synthesis in embedded hardware-software systems (poster abstract)
M. Auguin, C. Belleudy and G. Gogniat 80

9 TripleS-a formal validation environment for functional specifications (poster abstract)
J.-P. Soininen, J. Saarikettu, V. Veijalainen and T. Huttunen 83

10 SOFHIA: a CAD environment to design digital control systems (poster abstract)
R.J. Machado, J.M. Fernandes and A.J. Proença 86

11 Compiling the language BALSA to delay insensitive hardware (poster abstract)
A. Bardsley and D. Edwards 89

12 High-level synthesis of structured data paths (poster abstract)
C. Mandal and R.M. Zimmer 92

PART THREE Formal Characterizations of Systems 95

13 Characterizing a portable subset of behavioural VHDL-93
K. Thirunarayan and R. Ewing 97

14 Algebra of communicating timing charts for describing and verifying hardware interfaces
B. Berkane, S. Gandrabur and E. Cerny 114

15 A formal proof of absence of deadlock for any acyclic network of PCI buses
F. Corella, R. Shaw and C. Zhang 134

PART FOUR Analog Languages 157

16 Behavioural modelling of sampled-data with HDL-A and ABSynth
V. Moser, H.-P. Amann and F. Pellandini 159

PART FIVE Languages in Design Flows 179

17 Hardware description languages in practical design flows
R. Camposano 181

18 VHDL generation from SDL specification
J.-M. Daveau, G. Fernandes Marchioro and A.A. Jerraya 182

19 Exploiting isomorphism for speeding up instance-binding in an integrated scheduling allocation and assignment approach to architectural synthesis
B. Landwehr, P. Marwedel, I. Markhof and R. Dömer 202

PART SIX Future Trends in Hardware Design 213

20 Verification of large systems in silicon (special talk)
C. Ussery and S. Curry 215

21 The Shall Design test Development model for hardware systems
M. Heuchling, W. Ecker and M. Mrva 240

22 Modular operational semantic specification of transport triggered architectures
J. Mountjoy, P. Hartel and H. Corporaal 260

PART SEVEN Formal Methods for Asynchronous and Distributed Systems 281

23 The world of I/O: a rich application area for formal methods (invited talk)
F. Corella 283

24 Abstract modelling of asynchronous micropipeline systems using Rainbow
H. Barringer, D. Fellows, G. Gough and A. Williams 285

25 A new partial order reduction algorithm for concurrent system verification (short talk)
R. Nalumasu and G. Gopalakrishnan 305

PART EIGHT VHDL 315

26 VHDL power simulator: power analysis at gate level
L. Kruse, D. Rabe and W. Nebel 317

27 Object oriented extensions to VHDL. the LaMI proposal
J. Benzakki and B. Djafri 334

Index of contributors 348

Keyword index 349