

# Table of Contents

## 34<sup>th</sup> Annual International Symposium on Microarchitecture — MICRO-34

Message from the General Chair .....	ix
Message from the Program Chairs.....	x
Committees .....	xi
Reviewers .....	xiii

### Keynote

Fifty Years of Microarchitecture .....	2
<i>H. Cragon</i>	

### Session 1: Novel Ideas

Skipper: A Microarchitecture for Exploiting Control-Flow Independence .....	4
<i>C. Cher and T. Vijaykumar</i>	
Performance Characterization of a Hardware Mechanism for Dynamic Optimization .....	16
<i>B. Fahs, S. Bose, M. Crum, B. Slechta, F. Spadini, T. Tung, S. Patel, and S. Lumetta</i>	
Using Variable-MHz Microprocessors to Efficiently Handle Uncertainty in Real-Time Systems.....	28
<i>E. Rotenberg</i>	
A Design Space Evaluation of Grid Processor Architectures .....	40
<i>R. Nagarajan, K. Sankaralingam, D. Burger, and S. Keckler</i>	

### Session 2: Memory Hierarchies

Reducing Set-Associative Cache Energy via Way-Prediction and Selective Direct-Mapping .....	54
<i>M. Powell, A. Agrawal, T. Vijaykumar, B. Falsafi, and K. Roy</i>	
A Code Decompression Architecture for VLIW Processors .....	66
<i>Y. Xie, W. Wolf, and H. Lekatsas</i>	
Direct Load: Dependence-Linked Dataflow Resolution of Load Address and Cache Coordinate .....	76
<i>B. Chung, J. Zhang, J. Peir, S. Lai, and K. Lai</i>	

### Session 3: Energy Efficient Architectures

Reducing Power Requirements of Instruction Scheduling through Dynamic Allocation of Multiple Datapath Resources .....	90
<i>D. Ponomarev, G. Kucuk, and K. Ghose</i>	
Exploiting VLIW Schedule Slacks for Dynamic and Leakage Energy Reduction .....	102
<i>W. Zhang, N. Vijaykrishnan, M. Kandemir, M. Irwin, D. Duarte, and Y. Tsai</i>	

Reducing Power with Dynamic Critical Path Information .....	114
<i>J. Seng, E. Tune, and D. Tullsen</i>	

Direct Addressed Caches for Reduced Power Consumption .....	124
<i>E. Witchel, S. Larsen, C. Ananian, and K. Asanović</i>	

## **Keynote**

Emerging Applications for the Connected Home .....	136
<i>A. Wolfe</i>	

## **Session 4: Modulo Scheduling**

Modulo Schedule Buffers .....	138
<i>M. Merten and W. Hwu</i>	

Graph-Partitioning Based Instruction Scheduling for Clustered Processors.....	150
<i>A. Aletà, J. Codina, J. Sánchez, and A. González</i>	

Modulo Scheduling with Integrated Register Spilling for Clustered VLIW Architectures .....	160
<i>J. Zalamea, J. Llosa, E. Ayguadé, and M. Valero</i>	

## **Session 5: Compilation**

Efficient Static Single Assignment Form for Predication.....	172
<i>A. Stoutchinin and F. de Ferriere</i>	

The Impact of If-Conversion and Branch Prediction on Program Execution on the Intel® Itanium™ Processor...	182
<i>Y. Choi, A. Knies, L. Gerke, and T. Ngai</i>	

Mapping Reference Code to Irregular DSPs within the Retargetable, Optimizing Compiler COGEN(T).....	192
<i>G. Gréwal and C. Wilson</i>	

## **Session 6: Superscalar Architectures**

Select-Free Instruction Scheduling Logic.....	204
<i>M. Brown, J. Stark, and Y. Patt</i>	

Dual Use of Superscalar Datapath for Transient-Fault Detection and Recovery.....	214
<i>J. Ray, J. Hoe, and B. Falsafi</i>	

A High-Speed Dynamic Instruction Scheduling Scheme for Superscalar Processors .....	225
<i>M. Goshima, K. Nishino, Y. Nakashima, S. Mori, T. Kitamura, and S. Tomita</i>	

Reducing the Complexity of the Register File in Dynamic Superscalar Processors.....	237
<i>R. Balasubramonian, S. Dwarkadas, and D. Albonesi</i>	

## **Session 7: Multimedia and Graphics**

Saving Energy with Architectural and Frequency Adaptations for Multimedia Applications.....	250
<i>C. Hughes, J. Srinivasan, and S. Adve</i>	

Enhancing Loop Buffering of Media and Telecommunications Applications using Low-Overhead Predication.....	262
<i>J. Sias, H. Hunter, and W. Hwu</i>	
Cool-Cache for Hot Multimedia.....	274
<i>O. Unsal, R. Ashok, I. Koren, C. Krishna, and C. Moritz</i>	
ZR: A 3D API Transparent Technology for Chunk Rendering .....	284
<i>E. Hsieh, V. Pentkovski, and T. Piazza</i>	
<b>Session 8: Multithreading and Value Prediction</b>	
Speculative Lock Elision: Enabling Highly Concurrent Multithreaded Execution .....	294
<i>R. Rajwar and J. Goodman</i>	
Dynamic Speculative Precomputation.....	306
<i>J. Collins, D. Tullsen, H. Wang, and J. Shen</i>	
Handling Long-latency Loads in a Simultaneous Multithreading Processor.....	318
<i>D. Tullsen and J. Brown</i>	
Correctly Implementing Value Prediction in Microprocessors that Support Multithreading or Multiprocessing.....	328
<i>M. Martin, D. Sorin, H. Cain, M. Hill, and M. Lipasti</i>	
Index of Authors .....	339