TABLE OF CONTENTS

Preface . . . . *xv*

CHAPTER 1 *The Time for SOI* *1*

1.1 Technology Scaling in VLSI **1**

1.2 The End of Moore's Law? **2**

1.3 The Case for PD-SOI **6**
1.3.1 Why Partially Depleted SOI? 6
1.3.2 Why SOI Now? 7

1.4 Summary **9**

CHAPTER 2 *SOI Device Structures* *13*

2.1 Introduction **13**

2.2 Wafer Fabrication **14**
2.2.1 SIMOX 14
2.2.2 Bonded SOI Wafers 16
2.2.3 Smart Cut 17

2.3 Patterning SOI regions **17**

2.4 Transistor Structures **18**
2.4.1 Partially Depleted FET Structure 19
2.4.2 Body Contacts 22

2.5 Diodes **24**

2.5.1 Poly Bounded or Gated Diodes 24

2.6 Resistors 25

2.7 Decoupling Capacitors 26

2.8 Summary 27

CHAPTER 3 *SOI Device Electrical Properties* 29

3.1 Introduction 29

3.2 SOI MOSFET's Junction Diode 30

3.3 Impact Ionization 32

3.4 Floating Body Effects 34
3.4.1 History Effect and Threshold Voltage Variability 34
3.4.2 The Body Potential Range 37
3.4.3 The Body-Charging / Device Wearout Connection 37
3.4.4 The "Kinks" 41
3.4.5 Elevated DIBL 43
3.4.6 Reduced Body Effect / Source Follower Action 44
3.4.7 Reduced Short Channel Effect 46
3.4.8 Bipolar Device Action 47
3.4.9 Lower Temperature Sensitivity 51
3.4.10 Backchannel Device 52

3.5 SOI MOSFET Modeling 53
3.5.1 DC Discrete Element Representation 53
3.5.2 AC Discrete Element Representation 54

3.6 Insulator-Related Effects 54
3.6.1 Self Heating 55

3.6.2 Diffusion Capacitance Reduction 57
3.6.3 Latch-Up Elimination 57
3.6.4 SER Improvement 59

3.7 Composite Responses 60
3.7.1 Device Leakage - 5 Mechanisms 60
3.7.2 Conservation of Charge 61
3.7.3 Other Parasitic Active Elements 62

3.8 Summary 64

CHAPTER 4 *Static Circuit Design Response 67*

4.1 Introduction 67

4.2 Parameters of Interest to Circuit Designers 67

4.3 First Switch vs. Second Switch 69

4.4 First Switch vs. Steady State 75

4.5 Static Circuit Response to SOI 76
4.5.1 Inverter Response 76
4.5.2 Noise Response for Inverters 79
4.5.3 NAND Gate Response 80

4.6 Passgate Circuit Response 84

4.7 Summary 92

CHAPTER 5 *Dynamic Circuit Design Considerations. 95*

5.1 Introduction 95

5.2 Dynamic Circuit Response........................96
5.2.1 Dynamic History Effect 96
5.2.2 Dynamic Charge Sharing 97
5.2.3 Miller Capacitance 99
5.2.4 Half-Latch / Keeper Device Sizing................101

5.3 Preferred Dynamic Design Practices..............102
5.3.1 Predischarging 103
5.3.2 Cross-coupling of Dynamic Inputs.................105
5.3.3 Reordered Inputs.................................105
5.3.4 Early Setup 107
5.3.5 Logic Remapping 107
5.3.6 Complex Domino 108
5.3.7 Dynamic Noise Suppression........................108

5.4 Keeping Dynamic SOI Problems in Perspective ...110
5.4.1 Bipolar Effects and Noise in the 2W AND-OR 111
5.4.2 Charge Sharing Effects and Noise in the 2W AND-OR112

5.5 Soft Errors in Dynamic Logic 113

5.6 Dynamic Logic Performance......................115

5.7 Conclusions 116

CHAPTER 6 *SRAM Cache Design Considerations . . 119*

6.1 Overview 119

6.2 Writing a Cell 120
6.2.1 Capacitive Discharge Current.....................121
6.2.2 CMOS Subthreshold Leakage 122
6.2.3 Diode and Bipolar Currents 123

6.3 **Reading a Cell** 123
6.3.1 Read Leakage 124
6.3.2 Sense Amplifier Bias 124
6.3.3 Read Sense-Amp Strobe Timing vs. Read Frequency . 128
6.3.4 Single Polarity SRAMS 129
6.3.5 Word Line History 130

6.4 **Cell Stability and Cell Bias** 131
6.4.1 Transfer Ratio 131
6.4.2 Mistracking 132
6.4.3 Self Heating 133
6.4.4 Body Bias 133
6.4.5 Supply Rail Droop 135
6.4.6 Body-to-Body Coupling 135
6.4.7 Defect-Induced Bias 135
6.4.8 Passive History Effects 136
6.4.9 Making Sense of All This Bias! 137

6.5 **SRAM Noise Considerations** 138

6.6 **Precharging Circuitry** 140

6.7 **Soft Error Upsets** 141

6.8 **Array Test in PD-SOI** 145

6.9 **Summary** 146

CHAPTER 7 *Specialized Function Circuits in SOI . . 149*

7.1 **Introduction** 149

7.2 **Timing Elements** 149

7.3 Latch Response in SOI 153
7.3.1 Latch Stability and Noise.......... 153
7.3.2 Bipolar Charge Loss 154
7.3.3 Clock Skew due to History Effect 155

7.4 Input / Output Circuitry.......... 155
7.4.1 Clock Drivers 156
7.4.2 Data Drivers 156
7.4.3 Clock Receivers 157
7.4.4 Data Receivers 158
7.4.5 Voltage Reference.......... 158

7.5 Electro-Static Discharge (ESD) Protection.......... 158

7.6 Summary 161

CHAPTER 8 *Global Chip Design Considerations . . . 165*

8.1 Introduction.......... 165

8.2 Temperature Effects.......... 166
8.2.1 Design Considerations, Normal Operation.......... 166
8.2.2 Stress Considerations 167
8.2.3 Low Temperature Operation.......... 169

8.3 Noise Immunity.......... 175
8.3.1 Crosstalk (Capacitive Coupling).......... 176
8.3.2 Delay Noise.......... 176
8.3.3 Logic Noise.......... 177
8.3.4 Simultaneous Switching 178

8.4 Power Consumption 178

8.5 Power Supply Issues Noise.......... 185

8.6 System Performance 186

8.7 SOI Timing Variability. 187
8.7.1 Total Delay Variation 188
8.7.2 History Variation 189
8.7.3 Body Initialization. 190

8.8 Summary 191

CHAPTER 9 *Future Opportunities in SOI 195*

9.1 Introduction. 195

9.2 Floating Body Effect Suppression 196
9.2.1 Charge-Balanced Device Design 196
9.2.2 Field Shield Isolation 198
9.2.3 BESS. 199
9.2.4 Body-Linked Device. 200
9.2.5 Patterned Insulators. 201

9.3 DTCMOS 203
9.3.1 DTCMOS Low Voltage Static Logic 203
9.3.2 0.5V Pass-Gate Logic 205
9.3.3 DTCMOS Elevated Voltage Schemes 206

9.4 DGCMOS. 208

9.5 3-Dimensional SOI 209

9.6 Future Scaling Opportunities 210

9.7 Summary. 212

About the Authors. ccxxi